NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE & SYLLABUS
M.Tech for
VLSI & EMBEDDED SYSTEMS
PROGRAMME

Academic Regulations (R25) for M.Tech. (Regular)

(Effective for the students admitted into I year from the Academic Year 2025-2026 onwards)

ACADEMIC REGULATIONS - R25 FOR M.Tech (REGULAR) DEGREE COURSE

Applicable for the students admitted to M.Tech (Regular) Course from the Academic Year 2025-26 and onwards. The M.Tech Degree of Narasaraopeta Engineering College(Autonomous) affiliated to Jawaharlal Nehru Technological University Kakinada shall be conferred on candidates who are admitted to the program and who fulfil all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates (i) in national level qualifying Entrance Test (GATE), (ii) AP PGECET conducted by State Government and (iii) Few Sponsored seats notified by University on the basis of any order of merit as approved by the State Government /JNTUK University, Kakinada subject to reservations as laid down by the Government from time to time.

2.0 AWARD OF M.Tech DEGREE

2.1 A student shall be declared eligible for the award of the M.Tech Degree, if he pursues a course of study in not less than two and not more than four academic years. Under any circumstances, permission shall not be given to complete the course work beyond four years.

2.2 **The student shall register for all 80 credits and secure all the 80 credits.**

2.3 The minimum instruction period in each semester is 16 weeks.

3.0 PROGRAMME OF STUDY

The following specializations are offered at present for the M.Tech Programme of study.

M.Tech in

1. CSE/CS&E
2. Digital Electronics and Communication Systems
3. Digital Systems & Computer Electronics
4. Machine Design
5. Power and Industrial Drives
6. Structural Engineering
7. Thermal Engineering
8.VLSI & Embedded Systems

4.0 ATTENDANCE

4.1 Attendance is calculated separately for each course. Attendance in all classes (Theory/Laboratories) is compulsory. The minimum required attendance in each course is 75%. A student shall not be permitted to appear for the Semester End Examinations (SEE), if his/her attendance is less than 75%.

4.2 Condoning of shortage of attendance (between 65% and 75%) up to a maximum of 10% (*considering the days of attendance in sports, games, NSS activities and medical exigencies*) in each course (Theory/Lab/Seminar) is condoned on production of valid Certificates/documents in the stipulated time mentioned here

with:

4.2.1 Students who are admitted as in patients for treatment are only eligible to claim condonation of attendance. Such students under medical exigencies need to Produce (a) Doctor Medical Prescription, (ii) Medical bills duly signed by Doctor/Hospital authorities, (c) Diagnosis reports, if any, (d) Discharge summary issued at the time of discharge and any other supporting documents within two week(s) from the date of discharge.

Note: University at any point of time can inform the college to submit such list/proofs. *Hence, respective HOD shall verify and accord condonation privilege scrupulously*.

4.2.2 Students participation in Sports/Games and NSS activities shall also be permitted for condonation of attendance. In such cases, they need to produce (a) invitation letter from the organizing institute/agency, (ii) participation certificate and any supporting documents within two week(s) from the date of participation to the respective HOD.

4.3 A prescribed fee per course shall be payable for condoning shortage of attendance after getting the approval of College Academic Committee for the same. The College Academic Committee shall maintain all the relevant documents along with the request from the students, whose attendance is condoned.

4.4 Shortage of Attendance below 65% in any course shall in no case be condoned.

4.5 A Student, whose shortage of attendance is not condoned in any course(s) (Theory/Lab/Seminar) in any Semester, is considered as '**Detained in that course(s)**, and is not eligible to write Semester End Examination(s) of such Course(s), (in case of Seminar, his/her Seminar Report or Presentation are not eligible for evaluation) in that Semester; and he/she has to seek re-registration for those course(s) in subsequent Semesters, and attend the same as and when offered.

4.6 A student shall put in a minimum required attendance in at least FOUR courses in I semester for promotion to II Semester; and at least FOUR courses in II semester for promotion to III Semester.

Re-admission / re-registration

4.7 A student shall not be permitted to appear for the Semester End Examinations (SEE) in a course unless they meet the prescribed attendance requirements for that course. Such students may take readmission for the course in the subsequent semester when it is offered by paying the prescribed fee, *at least 30 days before the commencement of classwork*. The HOD concerned must obtain permission from the Principal by submitting the list of students eligible/applied for readmission before the commencement of classwork.

4.8 Students who fail due to **less internal marks (less than 50%)** may register for the course within the maximum permissible duration of the Program.

4.9 In such a case, the candidate must re-register for the course(s) and secure the required minimum attendance. The candidate's attendance in the re-registered course(s) shall be calculated separately to decide upon eligibility for writing the end examination in those course(s).

4.10 In a semester, students are permitted to re-register maximum of THREE courses.

4.11 Upon re-registration, the student's previous performance in the respective course(s) will be nullified. Re-registration must be completed by paying the prescribed fee at least 30 days prior to the commencement of classwork.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated course-wise, with a maximum of 100 marks for theory and 100 marks for practical, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory courses 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation. The continuous / internal evaluation shall be made based on the **average** of the marks secured in the two CIE/Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each CIE/midterm examination shall be conducted for a total duration of 120 minutes with 4 questions (without choice) each question for 10 marks. End semester examination is conducted for 60 marks for all FIVE (5) questions (one question from one unit) to be answered (either or).

5.2 For practical courses, 60 marks shall be awarded based on the performance in the End Semester Examinations and 40 marks shall be awarded based on the day-to-day performance as Internal Marks. The internal evaluation based on the day to day work-10 marks, record- 10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with breakup marks of Procedure-**15,** Experimentation- **25,** Results-10, Viva-voce-10.

5.3 For Seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to thedepartment in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other senior faculty members of the department. For Seminar, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 A candidate shall be deemed to have secured the minimum academic requirement in a course if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.5 Laboratory examination for M.Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher and the second examiner shall be drawn from the other autonomous colleges.

5.6 Students shall undergo mandatory summer internship / industrial training (credit Course) for a minimum of **eight weeks duration** at the end of second semester of the Programme/Summer Break. A student will be required to submit a summer internship/industrial training report to the concerned department and appear for an oral presentation before the committee. The Committee comprises of a HoD / Professor of the department and two faculty. The report and the oral presentation shall carry 40% and 60% weightages respectively. For summer internship / industrial training, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.7 The objective of comprehensive viva-voce is to assess the overall knowledge of the student in the relevant field of Engineering/Specialization in the PG program. Viva will be conducted in 3rd semester. The examination committee will be constituted by the HoD and consist of Professor of the department and two faculty. For comprehensive viva-voce, there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.0 EVALUATION OF SEMINAR/INTERNSHIP/DISSERTATION WORK

All the students admitted under these regulations have to mandatorily comply the requirements of (i) Seminar-I, (ii) Seminar-II, (iii) Comprehensive Viva, (iv) Dissertation Part-A and (v) Dissertation Part-B. Out of these, (i) to (iv) are evaluated by internally by Project Review Committee (PRC) and (v) External Evaluation.

6.1 A Project Review Committee (PRC) shall be constituted with Head of the Department and Two other senior faculty members in the department.

6.2 Students are required to appear for Seminar-I and Seminar-II in First and Second semester respectively. They shall present before PRC on the topic of their choice/interest preferably on the courses listed in respective semesters. PRC shall advise the students in advance to select topics which strengthen their Dissertation Part-A and Dissertation Part-B.

6.3 Registration of Dissertation/Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical and duly approved by PRC.

6.4 After satisfying 6.3, student has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval

6.5 If a candidate wishes to change his/her supervisor or topic of the project, he/she can do so with the approval of PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.6 Continuous assessment of Dissertation-Part A and Dissertation-Part B during the Semester(s) will be monitored by PRC. *Dissertation-Part A* will be only internal evaluation by PRC for 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

6.7 The candidate shall submit a status report to the PRC in two stages, each accompanied by an oral presentation, with a minimum interval of three months between the two.

6.8 The work on the project shall be initiated at the beginning of the III Sem and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis *(Dissertation – Part A & Part B)* only with the approval of PRC not earlier than 40 weeks from the date of registration of the project work.

6.9 Three copies of the project thesis, certified by the supervisor, shall be submitted to the PRC along with the plagiarism report.

6.10 The thesis shall be adjudicated by one examiner selected by the Principal. For this, the HOD of the concerned department shall submit a panel of 3 examiners, eminent in that field, with the help of the guide concerned.

6.11 If the report of the examiner is *not favourable*, the candidate shall revise and

resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is *not favourable* again, the thesis shall be summarily rejected. The candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the Principal.

6.12 If the report of the examiner is favourable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Head of the Department shall coordinate and make arrangements for the conduct of Viva-Voce examination. The Board shall jointly report the candidate's work for a maximum of 100 marks.

6.13 If the report of the Viva-Voce is unsatisfactory (i.e., < 50 marks), the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the Principal.

7.0 Cumulative Grade Point Average (CGPA)

Marks Range (Max – 100)	Letter Grade	Level	Grade Point
≥ 90	S	Outstanding	10
≥80 to <90	A	Excellent	9
≥70 to <80	B	Very Good	8
≥60 to <70	C	Good	7
≥50 to <60	D	Fair	6
<50	F	Fail	0
		Absent	0

Computation of SGPA

- The following procedure is to be adopted to compute the Semester Grade Point Average(SGPA) and Cumulative Grade Point Average(CGPA):
- The **SGPA** is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e

  SGPA (Si) = ∑ (Ci X Gi) / ∑ Ci
- Where Ci is the number of credits of the i^{th} course and Gi is the grade point scored by the student in the i^{th} course.

Computation of CGPA

- The **CGPA** is also calculated in the same manner taking into account all the courses undergone by a student over all the semester of a Programme, i.e.

  CGPA = ∑ (Ci X Si) / ∑ Ci
- Where Si is the SGPA of the i^{th} semester and Ci is the total number of credits in that semester.
- The SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.
- Equivalent Percentage = (CGPA- 0.5) x 10

8.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M.Tech. Degree he/she shall be placed in one of the following classes:

Class Awarded	CGPA to be secured	
First Division with Distinction	≥ 7.5 (without supplementary History)	From the CGPA secured from 80 credits
First Class	≥ 6.5	
Second Class	≥ 6.0 to < 6.5	

The secured grade, grade points, status and credits obtained will be shown separately in the memorandum of marks.

9.0 WITHHOLDING OF RESULTS

If the student is involved in indiscipline/malpractices/court cases, the result of the student will be withheld.

10.0 GENERAL

10.1 Wherever the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".

10.2 The academic regulation should be read as a whole for the purpose of any interpretation.

10.3 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

10.4 The College may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the College.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	**Punishment**
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.

3.	Impersonates any other candidate in connection with the examination.	Both the candidates involved in the malpractice will forefeit their seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.

6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat

8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or invigilators: Punishments to the candidates as per the above guidelines.

Programme Structure

R25 MTech (VLSI & ES) Structure

MTech (VLSI & ES) I – Semester

S. No.	Course Code	Course Title	L	T	P	C
1	PC	Advanced Digital Systems Design	3	1	0	4
2	PC	Embedded Hardware Platforms and Programming	3	1	0	4
3	PC	FPGA Design	3	1	0	4
4	PE-I	Program Elective-I	3	0	0	3
5	PE-II	Program Elective-II	3	0	0	3
6		Advanced Digital Systems Design Lab	0	1	2	2
7		Embedded Systems lab	0	1	2	1
8		Seminar-1	0	0	2	1
		Total	**15**	**5**	**6**	**23**

List of Professional Elective Courses in I Semester (Electives – I & II)

S.No.	Course Code	Course Title
1	PE -I	SCRIPTING LANGUAGES FOR VLSI
2	PE -I	VLSI Architectures
3	PE -I	VLSI System Design
4	PE -I	VLSI Testing & Testability
5	PE -II	System on Programming chip design
6	PE -II	Embedded system design using FPGA
7	PE -II	ARM Microcontroller based Design
8	PE -II	Cryptography and Network Security

@ Minimum 2/3 themes per elective

MTech (VLSI & ES) II – Semester

Sl. No.	Course Code	Course Title	L	T	P	C
1	PC	Digital CMOS Circuit Design	3	1	0	4
2	PC	System design with Embedded Linux	3	1	0	4
3	PC	Embedded Real Time Operating Systems (ERTOS)	3	1	0	4
4	PE-III	Program Elective-III	3	0	0	3
5	PE-IV	Program Elective-IV	3	0	0	3
6		Digital CMOS Circuit design lab	0	1	2	2
7		System Design with Embedded Linux Lab	0	1	2	2
8		Seminar-II	0	0	2	1
		Total	**15**	**5**	**6**	**23**

List of Professional Elective Courses in II Semester (Electives III & IV)

S.No.	Course Code	Course Title
1	PE -III	VLSI Signal processing
2	PE -III	Advanced VLSI Interconnects
3	PE -III	Quantum Computing
4	PE -III	VLSI Testing & Testability
5	PE -IV	System design using embedded Processors
6	PE -IV	Architectures for DSP
7	PE -IV	Internet of Things
8	PE -IV	Embedded Network and Protocols

@ Minimum 2/3 themes per elective

MTech (VLSI & ES) - III Semester

Sl. No.	Course Title	L	T	P	C
1	Research Methodology and IPR/Swayam 12 Week MOOC course- RM & IPR	3	0	0	3
2	Summer Internship/Industrial training (8- 10) Weeks*	-	-	-	3
3	Comprehensive Viva #	-	-	-	2
4	Dissertation part -A$	-	-	20	10
	Total	**3**	**-**	**20**	**18**

* Student attended during summer / year break and assessment will be done in 3rd Sem.
# Comprehensive viva can be conducted courses completed upto second sem.
$ Dissertation – Part A, internal assessment

MTech. (VLSI & ES) – IV Semester

Sl. No.	Course Title	L	T	P	C
1	Dissertation Part – B%	-	-	32	16
	Total	**-**	**-**	**32**	**16**

% External Assessment

Revised Bloom's Taxonomy Action Verbs

Definitions	I. Remembering	II. Understanding	III. Applying	IV. Analyzing	V. Evaluating	VI. Creating
Bloom's Definition	Exhibit memory of previously learned material by recalling facts, terms, basic concepts, and answers.	Demonstrate understanding of facts and ideas by organizing, comparing, translating, interpreting, giving descriptions, and stating main ideas.	Solve problems to new situations by applying acquired knowledge, facts, techniques and rules in a different way.	Examine and break information into parts by identifying motives or causes. Make inferences and find evidence to support generalizations.	Present and defend opinions by making judgments about information, validity of ideas, or quality of work based on a set of criteria.	Compile information together in a different way by combining elements in a new pattern or proposing alternative solutions.
Verbs	• Choose • Define • Find • How • Label • List • Match • Name • Omit • Recall • Relate • Select • Show • Spell • Tell • What • When • Where • Which • Who • Why	• Classify • Compare • Contrast • Demonstrate • Explain • Extend • Illustrate • Infer • Interpret • Outline • Relate • Rephrase • Show • Summarize • Translate	• Apply • Build • Choose • Construct • Develop • Experiment with • Identify • Interview • Make use of • Model • Organize • Plan • Select • Solve • Utilize	• Analyze • Assume • Categorize • Classify • Compare • Conclusion • Contrast • Discover • Dissect • Distinguish • Divide • Examine • Function • Inference • Inspect • List • Motive • Relationships • Simplify • Survey • Take part in • Test for • Theme	• Agree • Appraise • Assess • Award • Choose • Compare • Conclude • Criteria • Criticize • Decide • Deduct • Defend • Determine • Disprove • Estimate • Evaluate • Explain • Importance • Influence • Interpret • Judge • Justify • Mark • Measure • Opinion • Perceive • Prioritize • Prove • Rate • Recommend • Rule on • Select • Support • Value	• Adapt • Build • Change • Choose • Combine • Compile • Compose • Construct • Create • Delete • Design • Develop • Discuss • Elaborate • Estimate • Formulate • Happen • Imagine • Improve • Invent • Make up • Maximize • Minimize • Modify • Original • Originate • Plan • Predict • Propose • Solution • Solve • Suppose • Test • Theory

I Semester	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Exposes the design approaches using FPGAs.	K2
CO2	Provide in depth understanding of Fault models.	K4
CO3	Understands test pattern generation techniques for fault detection	K2
CO4	Design fault diagnosis in sequential circuits	K5
CO5	Provide understanding in the design of flow using case studies	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	H	L	H
CO2	M	L	H	M	L	L
CO3	H	M	H	M	M	L
CO4	H	M	H	M	M	L
CO5	H	M	H	M	L	M

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus	Contact Hours
UNIT- I	Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, FPGAs-FPGA technology, architecture, virtex CLB and slice, FPGA Programming Technologies, Xilinx XC2000, XC3000, XC4000 Architectures, Actel ACTI, ACT2 and ACT3 Architectures.	12
UNIT-II	Analysis and derivation of clocked sequential circuits with state graphs and tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. Need and Design strategies for multi-clock sequential circuits.	12
UNIT-III	Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Controller (FSM) Metastability, Synchronization, FSM Issues, Pipelining resources sharing, Sequential circuit design using FPGAs,	12

	Simulation and testing of Sequential circuits, Overview of computer Aided Design.	
UNIT-IV	Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model. Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing transition count testing, signature analysis and test bridging faults.	12
UNIT-V	Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment.	12
	Total	60

TEXT BOOKS:

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier Publications.
2. Fundamentals of Logic Design-Charles H. Roth, Jr. -5thEd., Cengage Learning.
3. Digital Circuits and Logic Design-Samuel C.LEE,PHI, 2008.

REFERENCE B0OKS:

I. Logic Design Theory-N.N. Biswas, PHI.
2. Digital System Design using programmable logic devices- Parag K. Lala, BS publications.
3. Switching and Finite Automata Theory -Zvi Kohavi & Niraj K. Jha, 3rd Edition, Cambridge,2010.

I Semester	EMBEDDED HARDWARE PLATFORMS AND PROGRAMMING	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Identify the functioning of embedded systems for different applications	K3
CO2	Develop embedded system programming skills	K4
CO3	Design, implement and test an embedded system	K5
CO4	Identify the unique characteristics of real-time embedded systems.	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	M	M	L
CO2	H	M	H	H	M	M
CO3	H	M	H	H	M	M
CO4	M	L	H	M	M	L

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus	Contact Hours
Unit I	Introduction to Embedded Computing: Embedded systems Overview, Characteristics of embedded computing applications, Design Challenges, Common Design Metrics, Processor Technology, IC Technology, Trade-offs.	12
Unit II	Process of Embedded System Development: The development process, Requirements, Specification, Architecture Design, Designing Hardware and Software components, system Integration and Testing.	12
Unit III	Hardware platforms: Types of Hardware Platforms, Single board computers, PC Add-on cards, custom-built hardware platforms, ARM Processor, CPU performance, CPU power consumption, Bus-based computer systems, Memory devices, I/O devices, component interfacing, Designing with microprocessors, system level performance analysis.	12
Unit IV	Program Design and Analysis: components for Embedded programs, Models of programs, Assembly, Linking, and loading, basic compilation techniques, software performance optimization, program level energy and Power analysis, Program validation and Testing.	12
Unit V	Real-Time Operating Systems: Architecture of the kernel, Tasks and Task Scheduler, Scheduling algorithms, Interrupt Service Routines, Semaphores, Mutex, Mailboxes, Message queues, Event Registers, Pipes, Signals,	12

	Timers, Memory management, Priority Inversion problem. Overview of off-the-shelf operating systems - MicroC/OS II, Vxworks, RT Linux.	
	Total	60

TEXT BOOKS:

1. Wayne Wolf: Computers as Components-Principles of Embedded Computer System Design, Morgan Kaufmann Publisher-2006, 2nd Edition
2. David E-Simon: An Embedded software Primer, Pearson Education, 2007, 1st Edition
3. K.V.K.K.Prasad Real-Time Systems: Concepts Design and Programming, Dreamtech Press, 2005

I Semester	FPGA DESIGN	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand FPGA design flow	
CO2	Identify the building blocks of commercially available FPGA/CPLDs	
CO3	Develop VHDL/Verilog models and synthesize targeting for Vertex, Spartan FPGAs	
CO4	Develop parameterized library cells and implement system designs using Parameterized	

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	H	M	H
CO2	M	L	H	M	L	M
CO3	H	M	H	H	M	H
CO4	H	M	H	H	M	H

(Please fill the above with Levels of Correlation, viz., L, M, H)

UNIT	SYLLABUS	CONTACT HOURS
UNIT - I	INTRODUCTION TO FPGAs: Evolution of programmable devices, FPGA Design flow, Applications of FPGA. DESIGN EXAMPLES USING PLDs: Design of Universal block, Memory, Floating point multiplier, Barrel shifter	12
UNIT - II	FPGAs/CPLDs: Programming Technologies, commercially available FPGAs, Xilinx's Vertex and Spartan, Actel's FPGA, Altera's FPGA/CPLD.	12
UNIT - III	Building blocks of FPGAs/CPLDs: Configurable Logic block functionality, Routing structures, Input/output Block, Impact of logic block functionality on FPGA performance, Model for measuring delay.	12
UNIT - IV	Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row – based FPGAs, introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures.	12

UNIT - V	FPGA architectural assumptions, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA CASE STUDY – Applications using Kintex-7, Virtex-7, Artix-7.	12
	Total	60

TEXT BOOKS:

1. John V. Old Field, Richrad C. Dorf, Field Programmable Gate Arrays, Wiley, 2008.
2. Data sheets of Artix-7, Kintex-7, Virtex-7
3. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, Field Programmable Gate Arrays, 2nd Edition, Springer, 1992.

I Semester	SCRIPTING LANGUAGES FOR VLSI	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Gain fluency in programming with scripting languages	K3
CO2	Create and run scripts using PERL/TCL/PYTHON in CAD Tools	K4
CO3	Demonstrate the use of PERL/PYTHON/ TCL in developing system and web applications	K4
CO4	Develop a real time project using PERL/PYTHON	K5

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	L	M	L
CO2	H	M	H	M	M	M
CO3	H	M	H	M	M	M
CO4	M	L	L	M	M	M

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus	Contact Hours
Unit I	Introduction to Scripts and Scripting: Basics of Linux, Origin of Scripting languages, scripting today, Characteristics and uses of scripting languages.	12
Unit II	PERL: Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.	12
Unit III	Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects and modules in action, Tied variables, interfacing to the operating systems, Security issues.	12
Unit IV	TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.	12
Unit V	Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, TCL and TK integration. PYTHON: Introduction to PYTHON language, PYTHON-syntax, statements,	12

	functions, Built-in functions and Methods, Modules in PYTHON, Exception Handling.	

TEXT BOOKS:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. PYTHON Web Programming, Steve Holden and David Beazley, New Riders Publications 12

REFERENCES:

1. TCL/TK: A Developer's Guide- ClifFlynt, 2003, Morgan Kaufmann Series.
2. Core PYTHON Programming, Chun, Pearson Education, 2006.
3. Learning Perl, Randal L. Schwartz, O' Reilly publications 6th edition 2011.
4. Linux: The Complete Reference", Richard Peterson McGraw Hill Publications, 6th Edition,2008.

I Semester	VLSI ARCHITECTURES	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	**Design RISC architecture and control units for a given instruction set.**	K5
CO2	**Improve the performance of RISC processors by applying pipelining Techniques**	K4
CO3	**Translate DSP algorithms into efficient hardware architectures and design associated building blocks**	K3
CO4	**Analyze the impact of retiming, unfolding, and folding on the performance of DSP architectures**	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	M	H	H	H	M
CO2	M	M	H	H	H	M
CO3	H	M	H	H	H	H
CO4	M	M	H	M	H	M

Unit	Syllabus	Contact Hours
Unit I	Instruction Set Architectures and CPU Performance: Overview of Instruction Set Architectures – CISC, RISC, and DSP Processors, CPU Performance and Its Factors, Evaluating Performance Metrics.	12
Unit II	Design of RISC Processor: Designing the Datapath and Control Unit for a RISC Processor, Multicycle Implementation of RISC Architecture.	12
Unit III	Enhancing Performance with Pipelining: Overview of Pipelining, Pipelined Datapath, Pipelined Control Unit, Pipeline Hazards – Data, Control, and Structural Hazards, Techniques for Hazard-Free Pipelined RISC Implementation.	12
Unit IV	Multiprocessors and DSP Algorithm Representation: Introduction to Multiprocessors, Multiprocessors Connected by a Single Bus and Network, Network Topologies, Evolution vs. Revolution in Computer Architecture, DSP Algorithm Representation – Data Flow Graphs, Loop Bound and Iteration Bound, Algorithms for Computing Iteration Bound.	12
Unit V	Pipelining, Parallel Processing, and VLSI Performance Techniques: Introduction to Pipelining and Parallel Processing, FIR Filter Pipelining, Parallel Processing Techniques, Pipelining and Parallel Processing for Low Power, VLSI Architecture Optimization Techniques – Retiming,	12

	Unfolding, and Folding.	
	Total	60

TEXT BOOKS:

1. D.A,Patterson And J.L.Hennessy, Computer Organization and Design: Hardware/ Software Interface, Elsevier, 2011, 4th Edition
2. Keshab Parhi, VLSI digital signal processing systems design and implementations, Wiley 1999

I Semester	VLSI SYSTEM DESIGN	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Model the behaviour of a MOS Transistor	
CO2	Understanding CMOS Inverter	
CO3	Design combinational and sequential circuits using CMOS gates	
CO4	Identify the sources of power dissipation in a CMOS circuit.	
CO5	Analyze SRAM cell and memory arrays	

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	M	L	L
CO2	M	L	H	M	M	M
CO3	H	M	H	M	H	M
CO4	H	M	H	M	H	M
CO5	H	M	H	M	M	L

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus	Contact Hours
Unit I	MOS Transistors, CMOS Logic, CMOS Fabrication and Layout, Design Partitioning, Fabrication, Packaging,and Testing, MOS transistor Theory, Long Channel I-V Characteristics, C-V Characteristics, Non-Ideal I-V Effects, DC Transfer Characteristics. The CMOS Inverter: The Static CMOS Inverter - An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Performance of CMOS Inverter: The Dynamic Behavior.	12
Unit II	CMOS Processing Technology, CMOS Technologies, Layout Design Rules, CMOS Process Enhancements, Technology-Related CAD Issues, Manufacturing Issues, Circuit Simulation- A SPICE Tutorial, Device Models, Device Characterization, Circuit Characterization, Interconnect Simulation. Combinational Circuit Design, Circuit Families, Silicon-On-Insulator Circuit Design, Sub Threshold Circuit Design, Sequential Circuit Design, Circuit	12

	Design of Latches and Flip-Flops, Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers, Wave Pipelining.	
Unit III	Power, Sources of Power Dissipation, Dynamic Power, Static Power, Energy-Delay Optimization, Low Power Architectures, Robustness, Variability, Reliability, Scaling, Statistical Analysis of Variability, VariationTolerant Design. Delay, Transient Response, RC Delay Model, Linear Delay Model, Logical Effort of Paths, Timing Analysis Delay Models, Datapath Subsystems, Addition/Subtraction, One/Zero Detectors, Comparators, Counters, Boolean Logical Operations, Coding, Shifters, Multiplication.	12
Unit IV	Array Subsystems, SRAM, DRAM, Read-Only Memory, Serial Access Memories, Content-Addressable Memory, Programmable Logic Arrays, Robust Memory Design, Special-Purpose Subsystems.	12
Unit V	CMOS Testing-The need for testing, Manufacturing test principles, Design strategies for test, Chip level test techniques, System level test techniques, Layout design for improved testability.	12
	Total	60

TEXT BOOKS:

1. Neil H.E. Weste, David Harris, Ayan Banerjee, CMOS VLSI Design – A Circuits and Systems Perspective, Pearson Education, 2006, 3rd Edition.
2. Neil H. E. Weste Kamran Eshraghian, Principles of CMOS VLSI DESIGN:A Systems Perspective, Pearson Education, 2006, 2nd Edition.

REFERENCE BOOKS:

1. Jan M RABAEY, Digital Integrated Circuits, Pearson Education, 2003, 2nd Edition.
2. Douglas A. Pucknell, Kamran Eshraghian, Basic VLSI Design, PHI,1994, 3 rd Edition.

I Semester	VLSI TESTING & TESTABILITY	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Identify the significance of testable design	K3
CO2	Understand the concept of yield and identify the parameters influencing the same	K2
CO3	Specify fabrication defects, errors, and faults	K3
CO4	Implement combinational and sequential circuit test generation algorithms	K4
CO5	Identify techniques to improve fault coverage	K5

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	L	L	M	H	M	L
CO2	M	M	M	H	H	M
CO3	M	L	M	H	H	M
CO4	M	M	M	H	M	H
CO5	M	L	M	H	H	M

Unit	Syllabus	Contact Hours
UNIT I	Role of Testing in VLSI Design Flow, Testing at Different Levels of Abstraction, Fault, Error, Defect, Diagnosis, Yield. Types of Testing, Rule of Ten, Defects in VLSI Chip. Modelling Basic Concepts, Functional Modelling at Logic Level and Register Level, Structure Models, Logic Simulation, Delay Models. Various Types of Faults, Fault Equivalence and Fault Dominance in Combinational and Sequential Circuits.	12
UNIT II	Fault Simulation Applications, General Fault Simulation Algorithms: Serial and Parallel, Deductive Fault Simulation Algorithms.	12
UNIT III	Combinational Circuit Test Generation, Structural Vs Functional Test, ATPG, Path Sensitization Methods. Difference Between Combinational and Sequential Circuit Testing, Five and Eight Valued Algebra, Scan Chain-Based Testing Method.	12
UNIT IV	D-Algorithm Procedure, Problems. PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN Algorithm. Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-Hoc Design, Generic Scan-Based Design.	12
UNIT	Classical Scan-Based Design, System Level DFT Approaches. Test Pattern	12

V	Generation for BIST, Circular BIST, BIST Architectures. Testable Memory Design: Test Algorithms, Test Generation for Embedded RAMs.	
	Total	60

TEXT BOOKS:

1. M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press, 1990.
2. M. Bushnell and V. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.

REFERENCE BOOKS:

1. Stroud,"A Designer's Guide to Built-in Self-Test", Kluwer AcademicPublishers,2002
2. V.Agrawal and S.C.Seth, Test Generation for VLSI Chips, Computer Society Press. 1989

Other Suggested Readings:

1. NPTELCourses(https://archive.nptel.ac.in/courses/117/105/117105137/)

I Semester	SYSTEM ON PROGRAMMING CHIP DESIGN	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the fundamental concepts and components of System-on-Chip (SoC) design, including design flow, hardware/software partitioning, and applications.	K2
CO2	Analyze and compare processor architectures such as RISC, CISC, VLIW, Superscalar, and soft/firm/custom processors, with emphasis on instruction handling and memory integration	K4
CO3	Evaluate various interconnection mechanisms like on-chip buses (AMBA, Core Connect, Wishbone, Avalon) and Network-on-Chip (NoC) architectures including topologies, routing algorithms, and QoS strategies	K4
CO4	Apply IP-based design methodologies in SoC development, including IP classification, reuse, lifecycle, integration, and implementation using FPGA prototypes	K3
CO5	Design and assess SoC implementations and testing techniques, including IP integration, RTOS, EDA tools, test automation strategies, and P1500 wrapper standardization	K5

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	M	L	L
CO2	H	M	H	M	M	M
CO3	H	M	H	M	H	M
CO4	H	M	H	H	M	M
CO5	H	M	H	H	M	H

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus	Contact Hours
Unit I	Introduction: Driving Forces for SoC - Components of SoC - Design flow of SoC Hardware/Software nature of SoC - Design Trade-offs - SoC Applications. System-level Design: Processor selection - Concepts in Processor Architecture: Instruction set architecture (ISA), elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom-Designed processors- on-chip memory.	12
Unit II	Interconnection: On-chip Buses: basic architecture, topologies, arbitration	12

	and protocols, Bus standards: AMBA, CoreConnect, Wishbone, Avalon - Network-on-chip: Architecture- topologies-switching strategies - routing algorithms flow control, Quality-of-Service- Re-configurability in communication architectures.	
Unit III	IP based system design: Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse – IP integration - IP evaluation on FPGA prototypes.	12
Unit IV	SOC implementation: Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design.	12
Unit V	SOC testing: Manufacturing test of SoC: Core layer, system layer, application layer - P1500 Wrapper Standardization - SoC Test Automation (STAT).	12
	Total	60

TEXT BOOKS:

1. Michael J.Flynn,WayneLuk,"Computer system Design: Systemon- Chip",Wiley-India, 2012.
2. Sudeep Pasricha, NikilDutt,"On Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
3. W.H.Wolf, "Computers as Components: Principles of Embedded Computing System Design", Elsevier, 2008.

REFERENCE BOOKS:

1. Patrick Schaumont "A Practical Introduction to Hardware/Software Co-design", 2ndEdition, Springer, 2012.
2. Lin, Y-L.S. (ed.), "Essential issues in SOC design: designing complex systems-on-chip. Springer, 2006.
3. Wayne Wolf, "Modern VLSI Design: IP Based Design", Prentice-Hall India, Fourth edition, 2009.

I Semester	EMBEDDED SYSTEM DESIGN USING FPGA	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Explain the architecture of embedded systems and identify the role of FPGAs and SoCs in modern VLSI-based platforms	K2
CO2	Develop and simulate digital circuits using VHDL/Verilog and design high-quality modular systems based on control flow graphs and abstraction Principles	K4
CO3	Demonstrate the ability to select and integrate system software, cross-development tools, boot-loaders, and monitors in FPGA-based embedded platforms	K3
CO4	Analyze partitioning strategies and communication mechanisms to optimize performance, resource usage, and system scalability	K4
CO5	Apply principles of spatial parallelism and identify contemporary design issues to build efficient, high-performance FPGA-based solutions	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	M	L	H
CO2	H	M	H	H	M	H
CO3	H	M	H	H	M	H
CO4	H	M	H	H	M	H
CO5	H	M	H	H	M	H

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus Content	Contact Hours
Unit I	Introduction to Embedded Systems and FPGA Platforms: Embedded System Overview: H/W-FPGA-Embedded SoC, Use of VLSI circuit technology, Platform FPGAs – Altera Cyclone, FPGA Platform, Components of platform FPGA systems, Adding custom compute cores, Assembling platform-based systems.	12
Unit II	Hardware Description and System Design: Hardware Description Languages: VHDL, Verilog, Other High-Level HDLs, HDL to Configuration Bit-stream generation. System Design using FPGA: Principles of system design, Design quality, Modules and interfaces, Abstraction and state, Cohesion and coupling, Design	12

	reuse strategies, Control flow graph, Origins of platform FPGA designs.	
Unit III	Software Design for FPGA Systems: Software Design Considerations: System Software Options, Root File System, Cross-Development Tools for Embedded Applications. Monitors and Boot-loaders: Role in platform-based development, Integration techniques.	12
Unit IV	Partitioning and Communication: Partitioning Overview: Partitioning Problem, Basic definitions, Expected performance gain, Resource considerations in partitioning, Analytical Approach to Partitioning. Scheduling and Communication: Invocation and coordination mechanisms, Transfer of state, Practical Issues in Profiling, Data structure design, Feature size manipulation.	12
Unit V	Parallelism and Contemporary Issues: Spatial Design Concepts: Principles of parallelism, Identifying parallelism in applications. Spatial Parallelism with Platform FPGAs: Within FPGA hardware cores, Across FPGA designs. Contemporary Issues in Embedded FPGA System Design: Trends, challenges, and emerging technologies.	12
	Total	60

Text Book(s):

1. Ron Sass, Andrew G. Schmidt, *Embedded Systems Design with Platform FPGAs: Principles and Practices*, First Edition, Tata McGraw Hill, India, 2011.

Reference Books:

1. Charles H. Roth Jr., *Digital Systems Design Using VHDL*, Reprint Edition, PWS Publishing Company (Thomson Books), USA, 2012.
2. V. A. Padroni, *Circuit Design with VHDL*, First Edition, MIT Press, Cambridge, England, 2011.
3. Wayne Wolf, *FPGA Based System Design*, First Edition, Prentice Hall, Modern Semiconductor Design Series, USA, 2011.

I Semester	ARM MICROCONTROLLER BASED DESIGN	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Explore the selection criteria of ARM processors by understanding the functional level tradeoff issues.	K2
CO2	Implementations on ARM developments towards the functional capabilities	K4
CO3	Work with ASM level program using the instruction set.	K2
CO4	Programming the ARM Cortex M.	K5
CO5	Discuss about Floating Point Operations:	K3

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	M	M	L
CO2	M	L	H	M	M	L
CO3	M	L	H	H	M	M
CO4	H	M	H	H	M	M
CO5	H	M	H	H	M	M

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit No.	Syllabus	Contact Hours
Unit I	**ARM Embedded Systems:** RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software. **ARM Processor Fundamentals:** Registers, CPSR, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families. **Architecture of ARM Processors:** Programmer's model, modes and states, special and floating-point registers, APSR, Memory system, MPU, Exceptions, NVIC, vector table, Fault handling, SCB, Debug, Reset sequence.	12

Unit II	**ARM Instruction Set:** Data processing, branch, load-store, software interrupt, program status register instructions, loading constants, ARMv5E extensions, Conditional execution. Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Branch, Data Processing, Load-Store, Stack, and Software Interrupt Instructions.	12
Unit III	**Technical Details of Cortex M Processors:** Overview of Cortex-M3 and M4: architecture, instruction set, block diagram, memory system, exception and interrupt support. Features: Performance, code density, low power, MPU, OS support, Cortex- M4-specific DSP features, Debug support, Scalability, Compatibility.	12
Unit IV	**Instruction Set of Cortex M:** Instruction set background, comparison across Cortex-M processors, UAL syntax, instruction suffixes, Cortex-M4-specific instructions, Barrel shifter, Special instructions and register access.	12
Unit V	**Floating Point Operations**: Floating point data and FPU overview (CPACR, FP registers, FPSCR, FPCCR, FPCAR, FPDSCR, MVFR0, MVFR1). DSP Applications: Dot product, Biquad filter, FIR, FFT and optimized DSP code writing for Cortex-M4.	12
	Total	60

TEXT BOOKS:

1. Andrew N.SLOSS, Dominic SYMES, Chris WRIGHT-ARM System Developer's Guide Designing and Optimizing System Software, Elsevier Publications, 2004.
2. Joseph Yiu, The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Elsevier Publications, 3rd Ed.,

REFERENCE BOOKS:

1. Steve Furber-Arm System on Chip Architectures–EdisonWesley,2000.
2. David Seal-ARM Architecture Reference Manual, EdisonWesley,2000.

I Semester	CRYPTOGRAPHY AND NETWORK SECURITY	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Identify and utilize different forms of crypto graphy techniques.	K3
CO2	In corporate authentication and security in the network applications.	K2
CO3	Distinguish among different types of threats to the system and handle the same	K4
CO4	Analyze Public-Key (Asymmetric) Cryptography and message digest algorithms	K2
CO5	Discuss about Authentication and System Security	K2

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	L	M	L
CO2	M	L	H	M	M	L
CO3	H	M	H	M	M	L
CO4	M	L	H	M	H	L
CO5	H	M	H	H	H	H

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus Content	Contact Hours
UNIT I	Security: Need, security services, Attacks, OSI Security Architecture, one-time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.	12
UNIT II	Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.	12
UNIT III	Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.	12
UNIT IV	Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4, MD5, Secure Hash algorithm, RIPEMD-160, HMAC.	12
UNIT V	Authentication and System Security: IP and Web Security, Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos,	12

	IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction, Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.	
	Total	60

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition

REFERENCE BOOKS:

1. Christopher M.King, Ertem Osmanoglu, Curtis Dalton,"Security Architecture, Design Deployment and Operations", RSA Press,
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

I Semester	ADVANCED DIGITAL SYSTEM DESIGN LAB	L	T	P	C
		0	1	2	2

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Design and simulate basic memory systems such as RAM and ROM using HDL	K5
CO2	Design and implement control units and data path logic for processor-like architectures	K5
CO3	Apply coding techniques like Hamming Code for error detection and correction	K3
CO4	Design and implement sequential digital systems using Finite State Machines (Mealy and Moore models).	K5
CO5	Develop and simulate real-time digital systems including UART communication, PWM generation, and digital clocks.	K4
CO6	Design and simulate application-oriented digital systems like vending machines, home alarm systems, and traffic controllers.	K5

Programming can be done using either VHDL /Verilog HDL. Download the programs on FPGA boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front-end tools and implement all the Designs in FPGA Kits.

List of Experiments:

1. Design of Memory (RAM and ROM).
2. Design of Control Unit and Data Processor Logic Design
3. Design and implementation of Hamming Code.
4. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
5. Design of DNA Sequence Detector
6. Design of Pulse Width Modulation
7. Design of UART Transmitter and Receiver Module
8. Design of Seven Segment Display
9. Design of Traffic Light Controller
10. Design and simulation ofHome Alarm System.
11. Design and simulation of Digital Clock.
12. Design and simulation of Vending Machine.

Lab Requirements:

I Semester	EMBEDDED SYSTEMS LAB	L	T	P	C
		0	1	2	2

Software required: Xilinx Vivado Tool.
Hardware required: Personal Computer, FPGA Development Board.

CO1	Demonstrate the ability to write and execute basic Embedded C programs on microcontroller platforms.	K4
CO2	Apply digital I/O interfacing techniques by programming ports to control and monitor external hardware.	K3
CO3	Implement timing-based operations using software and hardware delays, including loops and timers.	K4
CO4	Design embedded applications for real-time control scenarios such as traffic lights and alarms.	K5
CO5	Interface serial communication peripherals and measure real-time data over communication links	K4
CO6	Develop embedded software solutions for domain-specific applications such as industrial automation.	K5
CO7	Demonstrate the use of port headers and external devices (like LCDs and keypads) in an embedded system	K4

List of Experiments by using Embedded C

1. Write a simple program to print " Hello World"
2. Write a simple program to show a delay
3. Write a loop application to copy values from P1 to P2.
4. Write a C program for counting the no of times that a switch is pressed & released.
5. Write a simple program to create a portable hardware delay.
6. Write a C program to test loop time outs.
7. Write a C program to test hardware based timeouts loops.
8. Illustrate the use of port header file (PORT M) using an interface consisting of a keyword and Liquid crystal display.
9. Develop a simple EOS showing traffic light sequencing.
10. Write a program to display elapsed time over RS-232 Link.
11. Write a program to drive SEOS Using Timer 0.
12. Develop software for milk pasteurization system.
13. Develop & implement a program for intruder alarm system

II Semester	DIGITAL CMOS CIRCUIT DESIGN	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Analyze MOSFET behavior and CMOS inverter characteristics under static and dynamic conditions.	K4
CO2	Design various combinational and sequential logic blocks using CMOS technology.	K5
CO3	Optimize data path elements such as adders, multipliers, and barrel Shifters	K4
CO4	Design and evaluate memory architectures including SRAM and ROM Cells	K5
CO5	Interpret and implement circuit layouts using stick diagrams and layout Rules	K3

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO\PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	H	M	H	H	M	H
CO2	M	M	H	H	M	H
CO3	M	L	M	H	L	H
CO4	M	L	M	M	M	H
CO5	L	H	M	H	M	M

Unit	Syllabus	Contact Hours
UNIT I	**MOS Transistor Principles and CMOS Inverter**: MOSFET characteristics under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter – Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay Parameters, Stick Diagram and Layout Diagrams.	12
UNIT II	**Combinational Logic Circuits**: Static CMOS Design, Different Styles of Logic Circuits, Logical Effort of Complex Gates, Static and Dynamic Properties of Complex Gates, Interconnect Delay, Dynamic Logic Gates.	12
UNIT III	**Sequential Logic Circuits**: Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non-Bistable Sequential Circuits.	12
UNIT IV	**Arithmetic Building Blocks**: Data Path Circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs.	12

UNIT V	**Memory Architectures**: Memory Architectures and Memory Control Circuits: Read-Only Memories, ROM Cells, Read-Write Memories (RAM), Dynamic Memory Design, 6-Transistor SRAM Cell, Sense Amplifiers.	12
	Total	60

TEXT BOOKS:

1. JanRabaey, Anantha Chandrakasan, BNikolic,"Digital Integrated Circuits: A Design Perspective", Prentice Hall of India, 2nd Edition, Feb 2003
2. N.Weste,K.Eshraghian,"PrinciplesofCMOSVLSIDesign",AddisionWesley,2nd Edition, 1993

REFERENCE BOOKS:

1. MJ Smith, "Application Specific Integrated Circuits", Addisson Wesley,1997
2. Sung-MoKang &Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill,1998

II Semester	SYSTEM DESIGN WITH EMBEDDED LINUX	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Execute Linux and File I/O Commands.	K2
CO2	Analyze Kernel Architecture and Scheduler Features.	K3
CO3	Develop Device Drivers for various peripherals.	K4
CO4	Explore Linux Root File System and concepts of Embedded Linux.	K2
CO5	Analyze RT Linux Basics and OS Safety.	K3

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	L	M	L
CO2	H	M	H	H	M	M
CO3	H	M	H	H	M	H
CO4	M	M	H	M	H	M
CO5	M	M	H	H	H	M

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit No.	Syllabus	Contact Hours
UNIT I	**Overview of LINUX:** Introduction to UNIX/LINUX, LINUX Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec), Embedded LINUX Vs Desktop LINUX, Embedded LINUX Distributions.	12
UNIT II	**Linux Kernel:** Embedded Linux Architecture, Kernel Architecture, Hardware Abstraction Layer, Memory Manager, Scheduler, File System, I/O and Networking Subsystem, Inter Process Communication, User Space, and Start-up Sequence.	12
UNIT III	**Embedded Drivers:** Board Support Package: Embedded Storage, Memory Technology Devices (MTD), Embedded Drivers: Serial, I2C, USB, Ethernet, Timer, Kernel Modules, and Embedded File System.	12

UNIT IV	**Building and Debugging:** Kernel, Root File System, Case Studies: RTL LINUX, Micro C/OS-II, VxWorks, Embedded Linux, and Tiny OS.	12
UNIT V	**Linux Tasks:** Porting Applications, Real-Time Linux Basics, Kernel Priority, Task Creation, Print Commands, Compilation, Safety-Critical Features, Components, Programs.	12
	Total	60

TEXTBOOKS:

1. Chris Simmonds, "Mastering Embedded Linux Programming" - Second Edition, PACKT Publications Limited.

2. Karim Yaghmour, "Building Embedded Linux Systems", O'Reilly & Associates

3. P Raghvan, Amol Lad, Sriram Neelakandan, "Embedded Linux System Design and Development", Auerbach Publications

REFERENCE BOOKS:

1. Christopher Hallinan, "Embedded Linux Primer: A Practical Real-World Approach", Prentice Hall, 2nd Edition, 2010.

2. Derek Molloy, "Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition, 2014

II Semester	EMBEDDED REAL TIME OPERATING SYSTEMS	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Illustrate real time programming concepts.	K3
CO2	Apply RTOS functions to implement embedded applications	K3
CO3	Understand fundamentals of design consideration for embedded Applications	K2
CO4	Describe about the memory units and real time memory applications	K4
CO5	Discuss communication Common Design Problems	K3

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	L	L
CO2	H	M	H	H	M	M
CO3	H	L	H	H	M	M
CO4	M	L	H	M	H	L
CO5	H	M	H	H	H	H

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus Content	Contact Hours
UNIT I	Introduction to Real-Time Operating Systems: Defining an RTOS, The scheduler, Kernel Objects and services, Key characteristics of an RTOS. Task: Defining a Task, Task States and Scheduling, Typical Task Operations, Typical Task Structure, Synchronization, Communication and Concurrency.	12
UNIT II	Semaphores: Defining Semaphores, Typical Semaphore Operations, Typical Semaphore Use. Message Queues: Defining Message Queues, Message Queue States, Message Queue Content, Message Queue Storage, Typical Message Queue Operations, Typical Message Queue Use. Pipes, Event Registers, Signals and Condition Variables.	12
UNIT III	Exceptions and Interrupts: Exceptions and Interrupts, Applications of Exceptions and Interrupts, Closer look at exceptions and interrupts, Processing General Exceptions, Nature of Spurious Interrupts. Timer and Timer Services: Real-Time Clocks and System Clocks, Programmable Interval Timers, Timer Interrupt Service Routines.	12

	I/O Subsystems: I/O Concepts, I/O Subsystems.	
UNIT IV	Memory Management: Dynamic Memory Allocation in Embedded Systems, Fixed-Size Memory Management in Embedded Systems, Blocking vs. Non-Blocking Memory Functions, Hardware Memory Management Units. Modularizing an Application for Concurrency: An Outside-In Approach to Decompose Applications, Guidelines and Recommendations for Identifying Concurrency, Schedulability Analysis.	12
UNIT V	Synchronization and Communication: Synchronization, Communication, Resource Synchronization Methods, Critical Section, Common Practical Design Patterns, Specific Solution Design Patterns. Common Design Problems: Resource Classification, Deadlocks, Priority Inversion.	12
	Total	60

Text Books

1. Qing Li, Caroline Yao (2003), "Real-Time Concepts for Embedded Systems", CMP Books.

Reference Books

1. Albert Cheng, (2002), "Real-Time Systems: Scheduling, Analysis and Verification", Wiley Interscience.
2. Hermann Kopetz, (1997), "Real-Time Systems: Design Principles for Distributed Embedded Applications", Kluwer.
3. Insup Lee, Joseph Leung, and Sang Son, (2008) "Handbook of Real-Time Systems", Chapman and Hall.Krishna and Kang G Shin, (2001), "Real-Time Systems", McGraw Hill.

II Semester	VLSI SIGNAL PROCESSING	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the fundamentals of DSP systems, data flow modeling, and techniques like pipelining and parallel processing for FIR filters	K2
CO2	Apply retiming, unfolding, and algorithmic strength reduction techniques to optimize DSP architectures	K3
CO3	Analyze and implement pipelined and parallel processing architectures for IIR filters and fast convolution methods	K4
CO4	Design and evaluate bit-level arithmetic structures such as multipliers, FIR filters, and distributed arithmetic implementations	K5
CO5	Explore synchronous, wave, and asynchronous pipelining techniques and apply numerical strength reduction methods in DSP systems	K3

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	L	L	M	M	H	H
CO2	M	L	M	H	H	H
CO3	M	L	M	H	H	H
CO4	M	L	M	H	M	H
CO5	M	L	M	M	M	H

Unit	Syllabus	Contact Hours
UNIT I	Introduction to DSP: Typical DSP Algorithms, Benefits of DSP Algorithms, Representation of DSP Algorithms. Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.	12
UNIT II	Folding: Introduction, Folding Transform, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems. Unfolding: Introduction, Algorithm for Unfolding,	12

	Properties of Unfolding, Critical Path, Unfolding and Retiming, Applications of Unfolding.	
UNIT III	Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.	12
UNIT IV	Fast Convolution: Introduction, Cook-Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.	12
UNIT V	Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction Techniques, Power Estimation Approaches. Programmable DSP: Evaluation of Programmable DSPs, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.	12
	Total	60

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.

2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.

2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

II Semester	ADVANCED VLSI INTERCONNECTS	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Gain insight into transmission line parameters of VLSI interconnects.	K3
CO2	Understand novel and emerging solutions for future VLSI interconnect technologies.	K2
CO3	Analyze the impact of inductive effects in high-speed interconnects.	K4
CO4	Examine the influence of quantum effects in nanoscale interconnects.	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	H	H
CO2	M	L	M	H	H	H
CO3	M	L	M	H	H	H
CO4	M	L	M	H	H	H

Unit	Syllabus	Contact Hours
UNIT I	Introduction: Introduction to VLSI Interconnects, The Distributed RC Interconnect Model, Elmore Delay in Interconnects, Scaling Effects in Interconnects, Simulation and Delay Mitigation in RC Interconnects.	12
UNIT II	Inductive Effects: Inductive Effects in Interconnects, Distributed RLC Interconnect Model, Transmission Line Equations, When to Consider the Inductive Effects, Equivalent Elmore Model for RLC Interconnects, Two-Pole Model of RLC Interconnects from ABCD Parameters, RLC Interconnect Simulation.	12
UNIT III	Skin Effect and Electromigration: Origin of the Skin Effect, Effective Resistance at High Frequencies, Power Dissipation due to Interconnects, Electromigration in Interconnects, Mitigation of Electromigration.	12
UNIT IV	Crosstalk: Capacitive Coupling in Interconnects, Crosstalk Effects in Two Identical Interconnects, Mitigation Techniques, Analysis and Simulation of Coupled Interconnects. Extraction of Capacitance, Extraction of Inductance, Estimation of Interconnect Parameters from S-parameters	12
UNIT V	Quantum Effects: Quantum Conductance, Quantum Capacitance, Kinetic Inductance, Graphene Nanoribbon Interconnects, Analysis and Simulation	12

	of Interconnect Considering Quantum Effects.	
	Total	60

TEXT BOOKS:

1. Ashok K.Goel, High-SpeedVLSIInterconnects,2007.
2. Y.S.Diamand, Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications, 2009.

Reference Books:

1.H.SPhilip Wong and DejiAkinwande, Carbon nanotube and Graphene Device Physics,2011.

Other Suggested Readings:

NPTELCourses(https://onlinecourses.nptel.ac.in/noc22_ee125/preview

II Semester	QUANTUM COMPUTING	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the fundamental principles of quantum computation and the concept of qubits.	K2
CO2	Analyze multi-qubit systems and quantum communication protocols.	K4
CO3	Analyze multi-qubit systems and quantum communication protocols.	K4
CO4	Design and implement basic quantum algorithms and quantum circuits.	K5

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	H	L	H	L	M	L
CO2	H	M	H	M	M	M
CO3	H	M	H	M	L	M
CO4	H	M	H	H	M	H

Unit	Syllabus	Contact Hours
UNIT I	Review of Quantum Mechanics and Motivation for Quantum Computation. Qubit: The Qubit State - Matrix and Bloch Sphere Representation - Computational Basis - Unitary Evolution.	12
UNIT II	Multi-Qubit States: No-Cloning Theorem, Superdense Coding, Pure States to Bell States, Bell Inequalities. Protocols with Multi-Qubits: Swapping, Teleportation. Gates: CNOT, Toffoli Gate, NAND, FANOUT, Walsh-Hadamard.	12
UNIT III	Measurement: Projective Operators - General, Projective and POVM Measurement. Ensemble: Density Operators - Pure and Mixed Ensemble - Time Evolution - Post Measurement Density Operator. Composite Systems: Partial Trace, Reduced Density Operator, Schmidt Decomposition, Purification, Bipartite Entanglement.	12
UNIT IV	Quantum Computing: Classical Computing Using Qubits, Quantum Parallelism, Deutsch's Algorithm, Deutsch-Jozsa Algorithm.	12
UNIT V	Quantum Circuits: Basic Gates, ABC Decomposition, Gray Codes, Universal Gates, Principle of Deferred and Implicit Measurements. Quantum Fourier Transform and Applications: Phase Estimation, Order	12

	Finding, Factoring, Discrete Logarithm, Hidden Subgroup Problems. Role of Prime Factoring in Classical Cryptography. Search Algorithms, Quantum Error Correcting Codes, Physical Realization of Qubits.	
	Total	60

TEXT BOOKS:

1. M.A. Nielsen and I.L Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 2010, 10th Anniversary Edition
2. Chris Bernhardt, Quantum Computing for Everyone, The MIT Press, 2019.
3. RayLaPierre , Introduction to Quantum Computing, Springer, 2021.

REFERENCE BOOKS:

1. Quantum Theory: Concepts and Methods, Asher Peres, Kluwer Academic Publishers,1993.
2. Venkateswaran Kasirajan, Fundamentals of Quantum Computing: Theory and Practice, Springer, 2021.

Other Suggested Readings:

1. NPTEL Courses (https://nptel.ac.in/courses/106106232

II Semester	VLSI TESTING & TESTABILITY	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Identify the significance of testable design	K3
CO2	Understand the concept of yield and identify the parameters influencing the Same	K2
CO3	Specify fabrication defects, errors, and faults	K3
CO4	Implement combinational and sequential circuit test generation algorithms	K4
CO5	Identify techniques to improve fault coverage	K5

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	L	L	M	H	M	L
CO2	M	M	M	H	H	M
CO3	M	L	M	H	H	M
CO4	M	M	M	H	M	H
CO5	M	L	M	H	H	M

Unit	Syllabus	Contact Hours
UNIT I	Role of Testing in VLSI Design Flow, Testing at Different Levels of Abstraction, Fault, Error, Defect, Diagnosis, Yield. Types of Testing, Rule of Ten, Defects in VLSI Chip. Modelling Basic Concepts, Functional Modelling at Logic Level and Register Level, Structure Models, Logic Simulation, Delay Models. Various Types of Faults, Fault Equivalence and Fault Dominance in Combinational and Sequential Circuits.	12
UNIT II	Fault Simulation Applications, General Fault Simulation Algorithms: Serial and Parallel, Deductive Fault Simulation Algorithms.	12
UNIT III	Combinational Circuit Test Generation, Structural Vs Functional Test, ATPG, Path Sensitization Methods. Difference Between Combinational and Sequential Circuit Testing, Five and Eight Valued Algebra, Scan Chain-Based Testing Method.	12
UNIT	D-Algorithm Procedure, Problems. PODEM Algorithm, Problems on	12

IV	PODEM Algorithm. FAN Algorithm, Problems on FAN Algorithm. Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-Hoc Design, Generic Scan-Based Design.	
UNIT V	Classical Scan-Based Design, System Level DFT Approaches. Test Pattern Generation for BIST, Circular BIST, BIST Architectures. Testable Memory Design: Test Algorithms, Test Generation for Embedded RAMs.	12
	Total	60

TEXT BOOKS:

3. M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press, 1990.
4. M. Bushnell and V. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.

REFERENCE BOOKS:

3. Stroud,"A Designer's Guide to Built-in Self-Test", Kluwer AcademicPublishers,2002
4. V.Agrawal and S.C.Seth, Test Generation for VLSI Chips, Computer Society Press. 1989

Other Suggested Readings:

1. NPTELCourses(https://archive.nptel.ac.in/courses/117/105/117105137/)

II Semester	SYSTEM DESIGN USING EMBEDDED PROCESSORS	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Understand the fundamental concepts, architecture, and application areas of embedded systems along with development tools	K2
CO2	Explain the ARM Cortex-M3 architecture, its instruction sets, and internal registers relevant to embedded system programming	K2
CO3	Analyze exception handling mechanisms, Nested Vectored Interrupt Controller (NVIC), and interrupt behavior in Cortex-M3	K4
CO4	Develop embedded programs using C and assembly language with CMSIS support, including interrupt and memory protection handling	K4
CO5	Apply knowledge of STM32L15xxx microcontroller architecture and peripherals in designing, debugging, and implementing embedded system applications	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	H	M	M
CO2	M	L	H	H	M	M
CO3	H	M	H	H	M	L
CO4	H	M	H	H	M	M
CO5	H	M	H	H	M	H

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus Content	Contact Hours
UNIT I	**Embedded Concepts:** Introduction to embedded systems, Application Areas, Categories of embedded systems, Overview of embedded system architecture, Specialties of embedded systems, Recent trends in embedded systems, Architecture of embedded systems, Hardware architecture, Software architecture, Application Software, Communication Software, Development and debugging Tools. **ARM Architecture:** Background of ARM Architecture, Architecture Versions, Processor Naming, Instruction Set Development, Thumb-2 and Instruction Set Architecture.	12

UNIT II	**Overview of Cortex-M3:** Cortex-M3 Basics: Registers, General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence. **Instruction Sets:** Assembly Basics, Instruction List, Instruction Descriptions. **Cortex-M3 Implementation Overview:** Pipeline, Block Diagram, Bus Interfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus.	12
UNIT III	**Exceptions:** Exception Types, Priority, Vector Tables, Interrupt Inputs and Pending Behavior, Fault Exceptions, Supervisor Call and Pendable Service Call. **NVIC:** Nested Vectored Interrupt Controller Overview, Basic Interrupt Configuration, Software Interrupts and SYSTICK Timer. **Interrupt Behavior:** Interrupt/Exception Sequences, Exception Exits, Nested Interrupts, Tail-Chaining Interrupts, Late Arrivals and Interrupt Latency.	12
UNIT IV	**Cortex-M3/M4 Programming:** Overview, Typical Development Flow, Using C, CMSIS (Cortex Microcontroller Software Interface Standard), Using Assembly. **Exception Programming:** Using Interrupts, Exception/Interrupt Handlers, Software Interrupts, Vector Table Relocation. Memory Protection Unit and Other Cortex-M3 Features: MPU Registers, Setting Up the MPU, Power Management, Multiprocessor Communication.	12
UNIT V	**Cortex-M3/M4 Microcontroller:** STM32L15xxx ARM Cortex M3/M4 Microcontroller: Memory and Bus Architecture, Power Control, Reset and Clock Control, STM32L15xxx Peripherals: GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART. **Development and Debugging Tools:** Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE), Logic Analyzer etc.	12
	Total	60

TEXT BOOKS:

1. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, Second Edition, Elsevier Inc. 2010.
2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK.
3. David Seal "ARM Architecture Reference Manual", 2001 Addison Wesley, England; Morgan Kaufmann Publishers

REFERENCES:

1. Steve Furber, "ARM System-on-Chip Architecture", 2nd Edition, Pearson Education
2. Cortex-M series-ARM Reference Manual
3. Cortex-M3 Technical Reference Manual (TRM)

II Semester	ARCHITECTURES FOR DSP	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Understand programmable DSP architectures and system-level design approaches.	K2
CO2	Analyze memory organization, instruction sets, and superscalar SISC processors	K4
CO3	Design and implement efficient data paths and pipelined logic structures	K5
CO4	Apply high-level synthesis techniques and low-power design strategies	K3
CO5	Utilize HDLs and prototyping tools for real-time DSP system development	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	L	M	L
CO2	M	L	H	M	M	L
CO3	H	M	H	H	M	M
CO4	M	M	H	H	M	M
CO5	H	M	H	M	M	H

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus	Contact Hours
UNIT I	Digital Signal Processors: The Programmable DSP Architecture, Top-Down Design of Dedicated DSPs, A Library-Based Systems Design Environment. Classification of Architectures: An Abstract Computing Machine, Optimization of performance, Interconnection between Functional Units	**12**
UNIT II	A Multi-level Classification, Data and Instruction Memories: SISC Architectures, Addressing Modes, External Interface Units. VLSI SISC Processors: The SISC Processor, Pipeline Controlling SISCs, Superscalar Processors	**12**
UNIT	Data Path Logic Design: Introduction, Synchronous Data Path Design,	**12**

III	Monolithic Arithmetic Circuits, Implementation of Pipeline	
UNIT IV	High level Synthesis (HLS) of Data Path, Low power Data Design, Floating Point Arithmetic. Rapid Prototyping: Introduction, High Level Languages (HLLs) in DSP	**12**
UNIT V	Hardware Description Languages (HDLs), Optimizing Compilers, DSP Prototyping Environment, Real-Time SISC Prototyping	**12**
	Total	60

Text Books:

1. Vijay.K.Madisetti,―VLSI Digital Signal Processors-An Introduction to Rapid Prototyping and Design Synthesis‖, IEEE Press, 1999.
2. Richard J.Higgins,―Digital Signal Processing in VLSI ‖,Prentice Hall,1990.
3. B.Venkata Ramani and M.Bhaskar, Digital Signal Processors, Architecture, Programming and Applications –TMH, 2004.

Reference Books:

1. Jonatham Stein, Digital Signal Processing ,John Wiley,2005.
2. Avtar Singhand S.Srinivasan, Digital Signal Processing–Thomson Publications,2004

II Semester	INTERNET OF THINGS	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Analyze and compare various IoT hardware platforms and networking components including Linux-based configurations	K4
CO2	Understand the fundamentals of networking, OSI model, and data communication concepts essential for IoT systems	K2
CO3	Explain IoT architecture, communication patterns, and protocol stacks such as 6LoWPAN with security considerations	K2
CO4	Develop IoT applications using web technologies, databases, and mobile development tools with attention to data privacy	K5
CO5	Evaluate advanced IoT use cases, sensor node integration, and the role of big data and Industry 4.0 in smart systems.	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	M	H	L
CO2	M	L	H	M	H	M
CO3	H	M	H	M	H	M
CO4	H	M	H	H	H	M
CO5	H	M	H	H	H	M

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus Content	Contact Hours
UNIT I	The IoT Networking Core: Technologies involved in IoT Development: Internet/Web and Networking Basics, OSI Model, Data transfer referred with OSI Model, IP Addressing, Point to Point Data transfer, Point to Multi Point Data transfer & Network Topologies, Sub-netting, Network Topologies referred with Web, Introduction to Web Servers, Introduction to Cloud Computing.	12
UNIT II	IoT Platform Overview: Overview of IoT supported Hardware platforms such as Raspberry Pi, ARM Cortex Processors, Arduino and Intel Galileo boards. Network Fundamentals: Overview and working principle of Wired Networking equipment – Routers, Switches; Overview and working principle of Wireless Networking equipment – Access Points, Hubs etc.	12

	Linux Network Configuration Concepts: Networking configurations in Linux, Accessing Hardware & Device Files interactions.	
UNIT III	IoT Architecture: History of IoT, M2M – Machine to Machine, Web of Things, IoT protocols. Applications: Remote Monitoring & Sensing, Remote Controlling, Performance Analysis. The Architecture: The Layering concepts, IoT Communication Pattern, IoT Protocol Architecture, The 6LoWPAN. Security aspects in IoT.	12
UNIT IV	IoT Application Development: Application Protocols. Back-end Application Designing: Apache for handling HTTP Requests, PHP & MySQL for data processing, MongoDB Object type Database, HTML, CSS & jQuery for UI Designing, JSON library for data processing, Security & Privacy during development. Application Development for Mobile Platforms: Overview of Android / iOS App Development tools.	12
UNIT V	Case Study & Advanced IoT Applications: IoT applications in home, infrastructures, buildings, security, industries, home appliances, and other IoT electronic equipment. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and Sensor Nodes and interfacing using any embedded target boards (Raspberry Pi / Intel Galileo / ARM Cortex / Arduino).	12
	Total	60

TEXT BOOKS:

1. 6LoWPAN: The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley
2. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. Ovidiu Vermesan, Dr. Peter Friess, River Publishers
3. Interconnecting Smart Objects with IP: The Next Internet, Jean-Philippe Vasseur, Adam Dunkels, Morgan Kuffmann

REFERENCES:

1. The Internet of Things: From RFID to the Next-Generation Pervasive Network ed Lu Yan, Yan Zhang, Laurence T. Yang, Huansheng Ning
2. Internet of Things (A Hands-on-Approach), Vijay Madisetti, Arshdeep Bahga
3. Designing the Internet of Things, Adrian Mc Ewen (Author), Hakim Cassimally
4. Asoke K Talukder and RoopaR Yavagal,"Mobile Computing," Tata Mc Graw Hill, 2010.

II Semester	EMBEDDED NETWORKS AND PROTOCOLS	L	T	P	C
		3	0	0	3

Course Outcomes: At the end of the course, student will be able to (Four to Six)

		Knowledge Level (K)#
CO1	Acquire knowledge on communication protocols of connecting Embedded Systems	K3
CO2	Master the design level parameters of USB and CAN bus protocols.	K2
CO3	Design Ethernet in Embedded networks considering different issues.	K5
CO4	Acquire the knowledge of wireless protocols in Embedded domain.	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO / PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	H	L	M	L
CO2	M	L	H	L	M	M
CO3	H	M	H	M	M	M
CO4	H	M	H	M	H	H

(Please fill the above with Levels of Correlation, viz., L, M, H)

Unit	Syllabus	Contact Hours
Unit I	Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols - RS232 standard – RS485 – Synchronous Serial Protocols - Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.	12
Unit II	USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets – Data flow types – Enumeration – Descriptors – PIC18 Microcontroller USB Interface – C Programs – CAN Bus – Introduction - Frames – Bit stuffing – Types of errors – Nominal Bit Timing – PIC microcontroller CAN Interface – A simple application with CAN.	12
Unit III	Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.	12
Unit IV	Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for	12

	Embedded Systems – Using FTP – Keeping Devices and Network secure.	
Unit V	Wireless sensor networks – Introduction – Applications – Network Topology – Localization – Time Synchronization – Energy efficient MAC protocols – SMAC – Energy efficient and robust routing – Data Centric routing.	12
	Total	60

TEXT BOOKS

1. Embedded Systems Design: A Unified Hardware/Software Introduction-Frank Vahid, Tony Givargis, John & Wiley Publications, 2002
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port-Jan Axelson, Penram Publications, 1996.

REFERENCE BOOKS

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series –Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete-Jan Axelson, Penram publications,2003.
3. Networking Wireless Sensors-Bhaskar Krishnama chari ,Cambridge press2005.

II Semester	DIGITAL CMOS CIRCUIT DESIGN LAB	L	T	P	C
		0	1	2	2

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Have the ability to explain the VLSI Design Methodologies using Mentor Graphics Tools	K3
CO2	Grasp the significance of various design logic Circuits in full-custom IC Design.	K4
CO3	Have the ability to explain the Physical Verification in Layout Extraction	K3
CO4	Fully Appreciate the design and analyze of CMOS Digital Circuits	K4
CO5	Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation	K5

List of Experiments:

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Mentor Graphics Tool/Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

II Semester	SYSTEM DESIGN WITH EMBEDDED LINUX LAB	L	T	P	C
		0	1	2	2

Course Outcomes:

CO1	Demonstrate the ability to interface sensors and actuators with microcontroller boards	K4
CO2	Develop applications using Raspberry Pi for real-time control of output devices and sensor monitoring	K3
CO3	Design embedded systems using Beagle Bone board for basic input/output operations and display interfacing	K4
CO4	Interface input devices and sensors with Embedded Linux boards and develop basic human-machine interaction applications	K5
CO5	Integrate sensors, actuators, and communication interfaces to build real-time embedded applications	K4
CO6	Demonstrate debugging and testing skills for verifying sensor data, controlling actuators, and troubleshooting embedded systems	K5

Using Arduino Board

1. Temperature and Humidity sensor
2. Soil moisture
3. Ultra sonic sound sensor to measure distance
4. IR Sensor

Using Raspberry PI

1. Servo motor
2. MQ2 Gas sensor
3. LCD
4. Relay

Using beagle bone boards

1. Led blinking
2. Seven segment display
3. LCD
4. Switch(buzzer)

Using embedded Linux Board

1. 4×4Matrix
2. Light dependent resistor