NARASARAOPETA
NEC ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE FILE

ELECTRONIC DEVICES AND CIRCUITS

(19BEC3TH02)

Academic year :2020-21

Year/Sem : II/I

Regulation :R19

Faculty Incharge: Mr.B.Srinivasa Rao

Faculty In-charge

HoD,ECE

HEAD OF THE DEPARTMENT
DEPT.OF ELECTRONICS AND COMMUNICATION ENGG.
NARASARAOPETA ENGINEERING COLLEGE
NARASARAOPET-522 601

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NARASARAOPETA
NEC ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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Signature of the Faculty Member

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NARASARAOPET-522 601

Institute Vision and Mission

Narasaraopeta Engineering College

(Autonomous)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

VISION AND MISSION OF THE INSTITUTE

Vision:

To emerge as a **Centre of excellence** in technical education with a blend of effective **student centric teaching learning** practices as well as **research** for the transformation of **lives and community**.

Mission:

M1: Provide the best class infrastructure to explore the field of engineering and research.

M2: Build a passionate and a determined team of faculty with student centric teaching, imbibing experiential, innovative skills.

M3: Imbibe lifelong learning skills, entrepreneurial skills and ethical values in students for addressing societal problems.

Programme Educational Objectives and Programme Specific Outcomes

NARASARAOPETA
NEC ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Vision and Mission of the Department

Vision:

To emerge as a **centre of excellence** in Electronics and Communication Engineering through **student centric education** and **research focus** to cater the current and future needs of **society**.

Mission:

M1: To provide best infrastructure for empowering the students with quality education to motivate them towards higher studies and **research**

M2: To provide qualified and experienced faculty for **student centric teaching** in order to mould the students as successful professionals in modern Electronics industry

M3: To inculcate leadership qualities, professional etiquette, **ethical values** and **social** responsibilities

Programme Educational Objectives:

PEO1: Demonstrate successful professional careers with strong fundamental knowledge in mathematics, science and engineering to meet real time requirements of industry.

PEO2: Learn continuously with a focus on advanced emerging trends in the field of ECE and allied to meet the societal needs.

PEO3: Pursue higher education leading to masters and research programmes for knowledge dissemination in profession.

Programme Specific Outcomes:

PSO1: Design and develop IoT applications using Raspberry Pi, Arduino and other advanced processors.

PSO2: Design and synthesize various circuits using latest hardware and EDA tools.

PSO3: Design and analyse modern communication systems to meet the present and future needs of industry with cost effective solutions.

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NARASARAOPETA ENGINEERING COLLEGE
NARASARAOPET-522 601

Program Outcomes

NARASARAOPETA ENGINEERING COLLEGE

(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

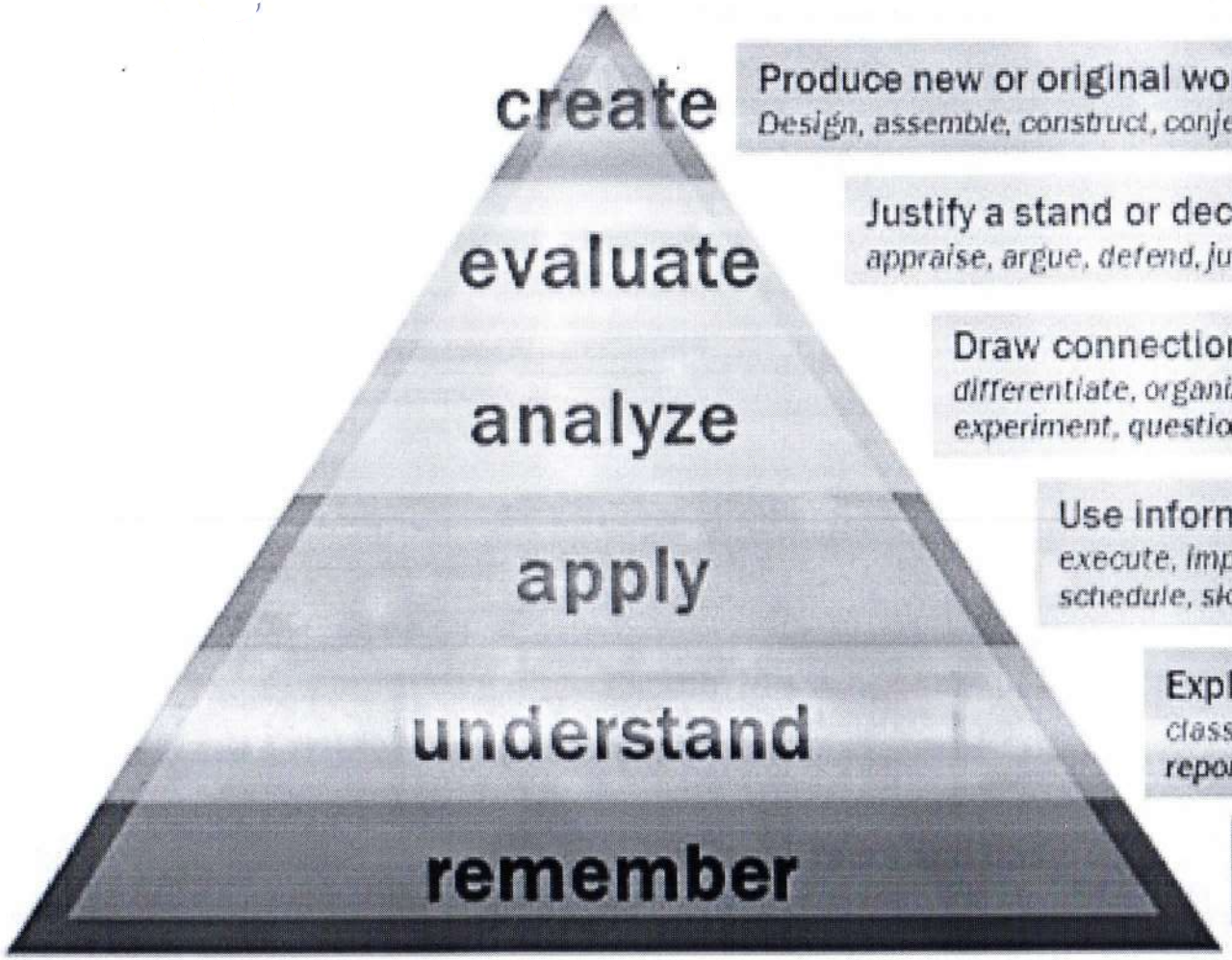
PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Bloom's Taxonomy levels

Bloom's Taxonomy



Produce new or original work
Design, assemble, construct, conjecture, develop, formulate, author, investigate

Justify a stand or decision
appraise, argue, defend, judge, select, support, value, critique, weigh

Draw connections among ideas
differentiate, organize, relate, compare, contrast, distinguish, examine, experiment, question, test

Use information in new situations
execute, implement, solve, use, demonstrate, interpret, operate, schedule, sketch

Explain ideas or concepts
classify, describe, discuss, explain, identify, locate, recognize, report, select, translate

Recall facts and basic concepts
define, duplicate, list, memorize, repeat, state

Course Objectives

&

Course Outcomes

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Year/Sem: II B.TECH I SEMESTER **Academic Year:** 2020-21

Course Name & Code: ELECTRONIC DEVICES AND CIRCUITS & 19BEC3TH02

COURSE OBJECTIVES:

1. Analyze the operation and principles of P-N diode.
2. Examine various types of Special diodes, rectifiers and filters.
3. Identify the working of BJT.
4. Analyze the need for transistor biasing and stabilization.
5. Identify the working of FET and other Transistors.

COURSE OUTCOMES:

After completion of the course, students will be able to

CO1: Use P-N diodes in electronic circuits.

CO2: Use special diodes and rectifiers in electronic circuits.

CO3: Explore the operation of BJT and its applications.

CO4: Analyse the thermal stability of BJT.

CO5: Explore the operation of FET, other transistors and their applications.

Signature of the Faculty Member

Course Information Sheet

NEC	**Narasaraopeta Engineering College** **(Autonomous)** **Yallmanda(Post), Narasaraopet- 522601** **DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

COURSE INFORMATION SHEET

PROGRAMME: B.Tech Electronics and Communication Engineering	
COURSE: **ELECTRONIC DEVICES AND CIRCUITS**	Semester : **I** CREDITS: **3**
COURSE CODE: 19BEC3TH02 REGULATION: **R19**	COURSE TYPE (CORE /ELECTIVE / BREADTH/ S&H): **CORE**
COURSE AREA/DOMAIN: **ELECTRONIC DEVICES**	PERIODS: **5** Per Week.

COURSE PRE-REQUISITES:

C.CODE	COURSE NAME	DESCRIPTION	SEM
	Engineering Physics	Knowledge of Free electron theory and Semiconductor Physics.	**I**
	Engineering Mathematics	Knowledge of Differentiation, Integration and Trigonometric Functions	**I**

COURSE OUTCOMES:

SNO	Course Outcome Statement
CO1	**Make Use of** P-N diodes in electronic circuits. **[K3]**.
CO2	**Make Use of** special diodes and rectifiers in electronic circuits. **[K3]**.
CO3	**Examine** the operation of BJT and its applications. **[K4]**.
CO4	**Analyze** the thermal stability of BJT. **[K4]**.
CO5	**Examine** the operation of FET, other transistors and their applications. **[K4]**.

SYLLABUS:

UNIT	DETAILS
I	**PN JUNCTION DIODE CHARACTERISTICS:** Insulators, Semiconductors and Metals–Classification using Energy gap, Intrinsic and Extrinsic Semiconductors. P-N Junction Diode - Formation of P-N Junction, Open Circuited P-N Junction, Biased P-N Junction - Forward Bias, Reverse Bias, Current Components in PN Junction Diode, Law of Junction, Diode Current Equation - Quantitative Analysis, V-I Characteristics of Diode - Forward Bias, Reverse Bias, Breakdown in P-N Junction Diode, Temperature Dependence on V-I Characteristics, Diode Resistance-Static Resistance, Dynamic Resistance, Reverse Resistance, Diode Capacitance - Transition Capacitance, Diffusion Capacitance, Energy Band Diagram of PN Junction Diode.
II	**SPECIAL DIODES AND RECTIFIERS:** Zener Diode - V-I Characteristics, Applications, Breakdown Mechanisms - Zener Breakdown and Avalanche Breakdown, Construction, Operation, Characteristics and applications of LED, LCD, Photodiode, Varactor Diode and Tunnel diode. **RECTIFIERS:** Basic Rectifier setup, Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Inductive and Capacitive Filters, L– Section and π- Section, Derive and compare rectifier parameters with and without filter.
III	**BIPOLAR JUNCTION TRANSISTOR (BJT):** Bipolar Junction Transistor – Types, Symbols and Operation, Transistor Current Components, Transistor Equation - Relation among IC, IB, ICBO, Transistor Configurations - CB, CE and CC, Transistor as a switch, Transistor switching times, Transistor as an Amplifier. Characteristics of Transistor in Common

	Base Configuration, Common Emitter and Common Collector Configurations - Input and output characteristics, Early effect, Transistor parameters, Current amplification factor, Relation among α, β, and γ, Comparison of CB, CE and CC Configurations, Punch Through/ Reach through, Typical transistor junction voltage values, Photo Transistor
IV	**BJT BIASING AND THERMAL STABILITY:** Need For Biasing, Operating Point, Load Line Analysis - D.C. Load Line, A.C. Load Line, Biasing - Methods, Basic Stability, Fixed Bias, Collector-to-base Bias and Self Bias, Stabilization against variations in VBE, Ic and β, Stability Factors S, S' and S'', Bias Compensation - Thermistor, Sensistor, Diode Compensation for variation in ICO, Thermal Runaway, Thermal Stability.
V	**FET & OTHER TRANSISTORS:** FET Types and Symbols - JFET and MOSFET/IGFET, JFET: N- Channel and P-Channel Construction, Operation, Characteristics - Drain and Transfer, Parameters - Drain Resistance, Amplification factor, Transconductance, Pinch-off voltage, MOSFET - Types - Depletion MOSFET - N Channel and P Channel, Enhancement MOSFET - N-Channel and P-Channel, Construction, Operation, Characteristics - Transfer and Drain Characteristics for Depletion and Enhancement Modes , Comparison between JFET and MOSFET.SCR- Symbol, Two-Transistor version, DIAC, TRIAC, UJT - Negative Resistance Property and Applications.

TEXT BOOKS	
T	**BOOK TITLE/AUTHORS/PUBLISHER**
T1	Electronic Devices and Circuits – J. Millman, C. Halkias, Tata McGraw-Hill, Third Edition, 2010.
T2	Electronic Devices and Circuits – Allen Mottershed, PHI, 2011.
T3	Electronic Devices and Circuits – Salivahanan, N. Suresh Kumar, A. Vallavaraj, Tata McGraw-Hill, Second Edition, 2008.
REFERENCE BOOKS	
R	**BOOK TITLE/AUTHORS/PUBLISHER**
R1	Integrated Electronics – Jacob Millman, C. Halkies, C.D. Parikh, Satyabrata Jit, Tata McGraw-Hill, Second Edition, 2011.
R2	Electronic Devices and Circuit Theory – R.L. Boylestad and Louis Nashelsky, Pearson Publications, Eleventh Edition, 2013.
R3	Electronic Devices and Circuits – A.P. Godse and U.A. Bakshi, Technical Publications, First Edition, 2009.

TOPICS BEYOND SYLLABUS/ADVANCED TOPICS:

SNO	DESCRIPTION	Associated PO & PSO
1	Overview of Semiconductors and Diodes	PO1,PO2,PO3, PSO1
2	Knowledge on Transistors	PO1,PO3, PO4, PSO1

WEB SOURCE REFERENCES:

1	Student Resources provided in https://www.electronics-tutorials.ws/ for basic electronic circuits
2	http://nptel.ac.in/courses/117105080/ on Electronics and Communication Engineering
3	http://www2.ece.ohio-state.edu/ee327/ Electronic Devices and Circuit laboratory
4	https://searchworks.stanford.edu/view/11352963 for fundamentals of Electronics available in Digital Library
5	https://electronicsforu.com/ for news on electronics and for Projects
6	https://archive.org/details/ElectronicDevicesCircuits
7	https://www.sanfoundry.com/1000-electronic-devices-circuits-questions-answers/ Question and Answers available on total Edc.

DELIVERY/INSTRUCTIONAL METHODOLOGIES:

☐Chalk & Talk	☐ PPT	☐Active Learning
☐Web Resources	☐ Students Seminars	☐Case Study
☐Blended Learning	☐ Quiz	☐Tutorials
☐Project based learning	☐NPTEL/MOOCS	☐ Simulation
☐Flipped Learning	☐Industrial Visit	☐Model Demonstration
☐Brain storming	☐Role Play	☐Virtual Labs

MAPPING CO'S WITH PO'S

CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2
C21 .1	3	3	1	2	-	-	-	-	-	-	-	2	3	2
C21.2	3	3	3	2	-	-	-	-	-	-	-	2	3	2
C21.3	3	3	2	2	-	-	-	-	-	-	-	2	3	1
C21.4	3	3	3	2	-	-	-	-	-	-	-	2	3	2
C21.5	2	3	2	2	-	-	-	-	-	-	-	2	2	2
Average	2.8	3	2.2	2	-	-	-	-	-	-	-	2	2.8	1.8

MAPPING COURSE WITH POs & PSOs

Course	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2	PSO 1	PSO 2
C21	3.00	3.00	2.25	2.00	-	-	-	-	-	-	-	2.00	3.00	1.75

COURSE OUTCOME RUBRIC (ASSESMENT PER STUDENT):					
ASSESMENT TOOL WITH WEIGHTAGE	**METHOD**	**ATTAINMENT LEVEL 3 (EXCELLENT)**	**ATTAINMENT LEVEL 2 (GOOD)**	**ATTAINMENT LEVEL 1 (AVERAGE)**	**ATTAINMENT LEVEL 0 (POOR)**
Internal tests (40%)	Direct	Student secured ≥ 60% marks of allocated marks for that CO	Student secured ≥ 60% and < 50% marks of allocated marks for that CO	Student secured ≥ 50% and <40% marks of allocated marks for that CO	Student secured < 40% marks of allocated marks for that CO
Assignments (20%)	Direct	Student secured ≥ 80% marks allocated for that CO	Student secured ≥ 70% and <80% marks allocated for that CO	Student secured ≥ 60% and <70% marks allocated for that CO	Student secured < 60% of marks allocated for that CO
End Semester Examination (30%)	Direct	Student secured grades A*&S* in External Exam	Student secured grades C*&B* in External Exam	Student secured grades D*&E* in External Exam	Student secured grades F* in External Exam
Course end Survey (10%)	Indirect	Student selected option	Student selected option	Student selected option	Student selected option
* Grade Definition: S: >= 90%; A: 80%-89%; B: 70%-79%; C: 60%-69%; D: 50%-59%; E: 40%-49%; F: <40%					

Course Coordinator **Module Coordinator** **Head of the Department**

HEAD OF THE DEPARTMENT
DEPT.OF ELECTRONICS AND COMMUNICATION ENGG.
NARASARAOPETA ENGINEERING COLLEGE
NARASARAOPET-522 601

ANNEXURE I:

(A) PROGRAM OUTCOMES(POs) Engineering Graduates will be able to:

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5.Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

(B) PROGRAM SPECIFIC OUTCOMES (PSOs) :

1. Analyze and design analog and digital circuits for a given specification and function.
2. Design a variety of electronic systems for applications including signal processing, communications, computer networks and control systems.

Cognitive levels as per Revised Blooms Taxonomy:

Cognitive Domain	LEVEL	Key words
Remember	K1	Defines, describes, identifies, knows, labels, lists, matches, names, outlines, recalls, recognizes, reproduces, selects, states.
Understand	K2	Comprehends, converts, defends, distinguishes, estimates, explains, extends, generalizes, gives an example, infers, interprets, paraphrases, predicts, rewrites, summarizes, translates.
Apply	K3	Applies, changes, computes, constructs, demonstrates, discovers, manipulates, modifies, operates, predicts, prepares, produces, relates, shows, solves, uses.
Analyse	K4	Analyzes, breaks down, compares, contrasts, diagrams, deconstructs, differentiates, discriminates, distinguishes, identifies, illustrates, infers, outlines, relates, selects, separates.
Evaluate	K5	Appraises, compares, concludes, contrasts, criticizes, critiques, defends, describes, discriminates, evaluates, explains, interprets, justifies, relates, summarizes, supports
Create	K6	Categorizes, combines, compiles, composes, creates, devises, designs, explains, generates, modifies, organizes, plans, rearranges, reconstructs, relates, reorganizes, revises, rewrites, summarizes, tells, write

Unit wise Sample assessment questions

COURSE OUTCOMES: Students are able to

CO 1: **Make Use of** P-N diodes in electronic circuits. **[K3].**

CO 2: **Make Use of** special diodes and rectifiers in electronic circuits. **[K3].**

CO 3: **Examine** the operation of BJT and its applications. **[K4].**

CO 4: **Analyze** the thermal stability of BJT. **[K4].**

CO 5: **Examine** the operation of FET, other transistors and their applications. **[K4].**

S NO	QUESTION	KNOWLEDGE LEVEL	CO
	UNIT I		
1	**List the PN diode** capacitances and solve capacitance for transition capacitance	K4	CO1
2	**Analyze** the Energy band Diagram of PN junction Diode.	K4	CO1
3	**Solve** the thermal voltage and barrier voltage at 250C , a Si PN junction is formed from P-material doped with 1022acceptors/m3 and n-material doped with 1.5 × 1021donors/m3 .	K3	CO1
4	**Analyze** VI characteristics of PN diode with Forward and Reverse bias.	K4	CO1
	UNIT 2		
1	**Analyze** Zener breakdown and Avalanche breakdown with briefly.	K4	CO2
2	**Analyze** the construction and working of LED.	K4	CO2
3	**Solve** the transformer secondary voltage for a capacitor input filter using a capacitance of 10p.F for a Full wave rectifier supplies a load requiring 300V at 200mA.	K3	CO2
4	**Analyze** the V-I Characteristic of Tunnel diode and explain its operation.	K4	CO2
	UNIT 3		
1	**Compare** α, β and γ of a transistor and also derive the relation among these.	K4	CO3
2	**Analyze** current components of transistor.	K4	CO3
3	**Solve** the IC ,IB ,β, and ICEO for a silicon, with α=0.995 emitter current is 10mA & leakage current IC0=0.5μA.	K3	CO3
4	**Compare** CB, CE & CC cofigurations.	K4	CO3
	UNIT 4		
1	**List** the advantage and disadvantages of fixed bias method.	K4	CO4
2	**Analyze** the working of collector – Base bias circuit using NPN transistor. Derive the equation for IB	K4	CO4
3	**Compare** the d.c and a.c load lines with suitable diagrams	K4	CO4
4	**Analyze** the working of Self Bias circuit using NPN transistor.	K4	CO4
	UNIT 5		
1	**Define** the Pinch-off voltage Vp. Sketch the depletion region before and after Pinch-off.	K1	CO5
2	**Explain** V-I characteristics of SCR with sketches?	K2	CO5
3	**Explain** briefly drain characteristics of N-channel enhancement MOSFET	K2	CO5
4	**Outline** the drain characteristics of a n-channel JFET and Explain it.	K2	CO5

❖

Model Question Paper- R19

Code: 19BEC3TH02

Narasaraopeta Engineering College(Autonomous)
Yallmanda(Post), Narasaraopet- 522601
II B. Tech I Semester Regular Examinations

ELECTRONIC DEVICES AND CIRCUITS

DEPARTMENT ELECTRONICS AND COMMUNICATION ENGINEERING

Time: 3 Hrs **Max. Marks: 60**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 12 marks.

		SECTION-I	**Cognitive Level**	**CO**	**Marks**
1	a	**Analyze** the V-I characteristics of PN junction diode in forward and reverse bias.	K4	CO1	[6M]
	b	**Analyze** the energy band diagram of PN junction diode.	K4	CO1	[6M]
		OR			
1	a	**Analyze** the Transition capacitance and diffusion capacitance of the Diode.	K4	CO1	[6M]
	b	**Solve** the silicon diode has reverse saturation current of 2.5uA at 300^0K. Find forward voltage for a forward current of 10mA.	K3	CO1	[6M]
		SECTION-II			
2	a	**Analyze** how a Zener diode works as a voltage regulator.	K4	CO2	[6M]
	b	**Analyze** the construction and working of LED.	K4	CO2	[6M]
		OR		CO2	
2	a	**Analyze** the construction and working of Varactor diode?	K4	CO2	[6M]
	b	**Analyze** ripple factor for L-Section filter connected to a full wave rectifier.	K4	CO2	[6M]
		SECTION-III			
3	a	**Compare** CE, CB and CC configurations.	K4	CO3	[6M]
	b	**Analyze** how transistor works as a Switch.	K4	CO3	[6M]
		OR			
3	a	**List** the different current components in a transistor and explain briefly.	K4	CO3	[6M]
	b	**Analyze** the phenomenon of early effect in transistors?	K4	CO3	[6M]
		SECTION-IV			

4	**a**	**Analyze** thethermal runaway? Derive necessary expressions to obtain thermal stability. **[6M]**	**K4**	**CO4**	**[6M]**
	b	**Analyze** the collector to base bias method in transistors?	**K4**	**CO4**	**[6M]**
		OR			
4	**a**	**Analyze** about Self Bias in a transistor.	**K4**	**CO4**	**[6M]**
	b	**Classify** the transistor load line analysis and explain it.	**K4**	**CO4**	**[6M]**
		SECTION-V			
5	**a**	**Analyze** the construction and operation of JFET.	**K4**	**CO5**	**[6M]**
		Analyze about Drain and Transfer Characteristics of Enhancement type N-channel MOSFET.	**K4**	**CO5**	**[6M]**
		OR			
5	**a**	**Compare** JFET and MOSFET.	**K4**	**CO5**	**[4M]**
	b	**Analyze** about i)Drain Resistance ii)Amplification factor iii) Transconductance iv) Pinch-off voltage	**K4**	**CO5**	**[8M]**
		**********			

II-Model Question Paper- R19

Code: 19BEC3TH02

Narasaraopeta Engineering College(Autonomous)
Yallmanda(Post), Narasaraopet- 522601
II B. Tech I Semester Regular Examinations
ELECTRONIC DEVICES AND CIRCUITS

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Time: 3 Hrs **Max. Marks: 60**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 12 marks.

*****

		SECTION-I	**Cognitive Level**	**CO**	**Marks**
	a	**Analyze** semiconductors, insulators and metals classification using energy band diagrams.	**K4**	**CO1**	**[6M]**
	b	**Solve** the current flowing through a Germanium Diode at room temperature is 8 x 10^{-7} amps when large reverse voltage is applied. Calculate the current flowing through the Diode when 0.1V forward bias is applied.	**K3**	**CO1**	**[6M]**
		OR			
1	**a**	**Examine** the working of an open circuited PN junction. Give necessary response curves.	**K4**	**CO1**	**[6M]**
	b	**Analyze** in detail about the current components in a PN junction diode.	**K4**	**CO1**	**[6M]**
		SECTION-II			
2	**a**	**Analyze** the construction and working of LCD.	**K4**	**CO2**	**[6M]**
	b	**Make use of** circuit and necessary waveforms explain the operation of bridge rectifier.	**K3**	**CO2**	**[6M]**
		OR			
2	**a**	**Analyze** the construction and working of Tunnel diode.	**K4**	**CO2**	**[6M]**
	b	**List** the rectifier and derive rectification efficiency expressions for it for the following (i) Half wave (ii) Full wave rectifier.	**K4**	**CO2**	**[6M]**
		SECTION-III			
3	**a**	**Analyze** input and output characteristics of a NPN transistor in CE configuration.	**K4**	**CO3**	**[6M]**
	b	**Compare** CE, CB and CC configurations.	**K4**	**CO3**	**[6M]**
		OR			
3	**a**	**Make use of** a neat diagram show different current components in a transistor.	**K3**	**CO3**	**[6M]**
	b	**Analyze** about Photo Transistor.	**K4**	**CO3**	**[6M]**

		SECTION-IV			
4	**a**	**Analyze** the voltage divider biasing method for BJT.	**K4**	**CO4**	**[6M]**
	b	**Solve** the silicon transistor with fixed bias, V_{CC} =9V, R_C =3 kΩ, R_B =8 kΩ, β=50, V_{BE}=0.7V.	**K3**	**CO4**	**[6M]**
		OR			
4	**a**	**Analyze** about Self Bias in a transistor.	**K4**	**CO4**	**[6M]**
	b	**Analyze** about basic stability of operating point in a transistor .	**K4**	**CO4**	**[6M]**
		SECTION-V			
5	**a**	**Analyze** the operation of N-channel enhancement type MOSFET with the help of it's ($I_D - V_{DS}$) and ($I_D - V_{GS}$) characteristics.	**K4**	**CO5**	**[6M]**
	b	**Analyze** about Construction, Operation and Characteristics of SCR.	**K4**	**CO5**	**[6M]**
		OR			
5	**a**	**Analyze** about Construction, Working of UJT.	**K4**	**CO5**	**[6M]**
	b	**Analyze** about Drain and Transfer characteristics of JFET with neat sketches.	**K4**	**CO5**	**[6M]**
		**********			

Academic calendar

Narasaraopeta Engineering College (Autonomous)
Kotappakonda Road, Yellamanda (P.O), Narasaraopet- 522601, Guntur District, AP.

ACADEMIC CALENDAR
(B.Tech. 2019, 2018 and 2017 admitted batches, Academic Year 2020-21)

2019 Batch 2nd Year 1st Semester, 2018 Batch 3rd Year 1st Semester and 2017 Batch 4th Year 1st Semester			
Description	**From Date**	**To Date**	**Duration**
Commencement of Class Work	02-11-2020		4 Weeks
1st Spell of Instructions	**02-11-2020**	**30-11-2020**	
I Mid examinations	01-12-2020	05-12-2020	1 Week
2nd Spell of Instructions	**07-12-2020**	**20-02-2021**	11 Weeks
II Mid examinations	22-02-2021	27-02-2021	1 Week
Preparation & Practicals	01-03-2021	06-03-2021	1 Week
Semester End Examinations	08-03-2021	20-03-2021	2 Weeks
2019 Batch 2nd Year 2nd semester, 2018 Batch 3rd Year 2nd Semester and 2017 Batch 4th Year 2nd Semester			
Commencement of Class Work	22-03-2021		7 Weeks
1st Spell of Instructions	**22-03-2021**	**08-05-2021**	
I Assignment Test	**12-04-2021**	**17-04-2021**	
II Assignment Test	**26-04-2021**	**30-04-2021**	
I Mid examinations	10-05-2021	15-05-2021	1 Week
2nd Spell of Instructions	**17-05-2021**	**03-07-2021**	7 Weeks
III Assignment Test	**31-05-2021**	**05-06-2021**	
IV Assignment Test	**21-06-2021**	**26-06-2021**	
II Mid examinations	05-07-2021	10-07-2021	1 Week
Preparation & Practicals	12-07-2021	17-07-2021	1 Week
Semester End Examinations	19-07-2021	31-07-2021	2 Weeks

PRINCIPAL

Time tables

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II Year, I Semester, ECE-A, Class Time Table for the A.Y. 2020-21

Room No.: 3301 w.e.f: 17-08-2020

DAY	1	2		3	4		5	6	7
	9:10 to 10:00	10:00 to 10:50	10:50 to 11:00	11:00 to 11:50	11:50 to 12:40	12:40 to 1: 30	1:30 to 2:20	2:20 to 3:10	3:10 to 4:00
MON	IoT	IOT LAB				LUNCH BREAK	EDC	S&S	NMCV
TUE	S&S	EDC	BREAK	DS	IoT		NMCV	DS	QA&R
WED	DS	S&S LAB					EDC	S&S	NMCV
THU	QA&R	EDC	BREAK	S&S	DS		NMCV	DS	IoT
FRI	NMCV	DS LAB					EDC	S&S	IoT
SAT	DS	EDC LAB					IoT	NMCV	S&S

NM&CV	: Numerical Methods & Complex Variables	Ms. J.Radhika
EDC	: Electronic Devices & Circuits	Dr. V. Venkata Rao
S&S	: Signals& Systems	Dr. SK.SD. Basha
IoT	: Internet of Things	Ms. J. Sravanthi
DS	: Data Structures	Mr. B.Satish Kumar
EDC Lab	: Electronic Devices & Circuits Lab	Mr.P.S.S.Chakravarthy Mr. T. Ravikanth Dr. T. Santhi Mr. P. Bhagya Raju Dr. Ayesha Mr. B. Srinivasa Rao Mr. N. Srinivasa Rao
S&S Lab	: Signals & Systems Lab	Dr. K. Raju Ms.D.Sai Chandrika Dr. SK.SD. Basha Dr.K.Laxma Reddy Mr. M. Srinivasa Rao
IoT Lab	: Internet of Things Lab	Ms. J. Sravanthi Mr. Sk. Zuber Basha Ms.D.Sai Chandrika Dr.T.R.Chandra Babu Dr. A.V.Nageswara Rao
DS Lab	: Data Structures Lab	Mr. B.Satish Kumar Ms. G.Prasanthi

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II Year, I Semester, ECE-B, Class Time Table for the A.Y. 2020-21

Room No.: 3302 w.e.f: 17-08-2020

DAY	1	2		3	4		5	6	7
	9:10 to 10:00	10:00 to 10:50	10:50 to 11:00	11:00 to 11:50	11:50 to 12:40	12:40 to 1: 30	1:30 to 2:20	2:20 to 3:10	3:10 to 4:00
MON	NMCV	S&S	BREAK	EDC	S&S	LUNCH BREAK	QA&R	IoT	DS
TUE	DS	IOT LAB					EDC	S&S	NMCV
WED	S&S	DS	BREAK	EDC	NMCV		IoT	DS	NMCV
THU	IoT	S&S LAB					EDC	S&S	DS
FRI	DS	EDC LAB					NMCV	EDC	QA&R
SAT	IoT	DS LAB					S&S	IoT	NMCV

NM&CV	: Numerical Methods & Complex Variables	Mr. D. Uma Shankar
EDC	: Electronic Devices & Circuits	Dr. T. Santhi
S&S	: Signals& Systems	Dr. K. Raju
IoT	: Internet of Things	Dr.T.R.Chandra Babu
DS	: Data Structures	Mr. B.Sateesh Kumar
EDC Lab	: Electronic Devices & Circuits Lab	Mr.P.S.S.Chakravarthy Dr. T. Santhi Dr. Ayesha Mr. T. Ravikanth Mr. B. Srinivasa Rao Mr. N. Srinivasa Rao Mr. P. Bhagya Raju
S&S Lab	: Signals & Systems Lab	Dr. K. Raju Mr. M. Srinivasa Rao Dr.K.Laxma Reddy Dr. SK.SD. Basha Ms.D.Sai Chandrika Dr. R. S. Siva Nayak
IoT Lab	: Internet of Things Lab	Ms. J. Sravanthi Dr.T.R.Chandra Babu Mr. Sk. Zuber Basha Ms.D.Sai Chandrika Dr. A.V.Nageswara Rao
DS Lab	: Data Structures Lab	Mr. B.Satish Kumar Ms. G.Prasanthi

HEAD OF THE DEPARTMENT
(Dr. V. VENKATA RAO)

PRINCIPAL

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II Year, I Semester, ECE-C, Class Time Table for the A.Y. 2020-21

Room No.: 3303 w.e.f: 17-08-2020

DAY	1	2		3	4		5	6	7
	9:10 to 10:00	10:00 to 10:50	10:50 to 11:00	11:00 to 11:50	11:50 to 12:40	12:40 to 1: 30	1:30 to 2:20	2:20 to 3:10	3:10 to 4:00
MON	NMCV	S&S	BREAK	QA&R	IoT	LUNCH BREAK	IOT LAB		
TUE	DS	IoT		EDC	QA&R		S&S	DS	NMCV
WED	NMCV	DS		S&S	IoT		S&S LAB		
THU	NMCV	S&S		EDC	DS		IoT	EDC	NMCV
FRI	IoT	EDC		DS	S&S		DS LAB		
SAT	NMCV	DS		S&S	EDC		EDC LAB		

NM&CV	: Numerical Methods & Complex Variables	Ms. J.Radhika
EDC	: Electronic Devices & Circuits	Mr.P.S.SChakravarthy
S&S	: Signals& Systems	Dr. R. S. Siva Nayak
IoT	: Internet of Things	Dr. A.V.Nageswara Rao
DS	: Data Structures	Mr. G. Prasanthi
EDC Lab	: Electronic Devices & Circuits Lab	Mr. T. Ravikanth Mr.P.S.S Chakravarthy Mr. B. Srinivasa Rao Mr. N. Srinivasa Rao Dr. Ayesha Dr. T. Santhi Mr. A. Ravindra Babu Mr. P. Bhagya Raju
S&S Lab	: Signals & Systems Lab	Dr. R. S. Siva Nayak Mr. M. Srinivasa Rao Dr.K.Laxma Reddy Ms.D.Sai Chandrika Dr. SK.SD. Basha
IoT Lab	: Internet of Things Lab	Dr.A.V.Nageswara Rao Ms.J.Sravanthi Ms.D.Sai Chandrika Dr.T.R.Chandra Babu
DS Lab	: Data Structures Lab	Ms.G.Prasanthi Mr. B.Sateesh Kumar

HEAD OF THE DEPARTMENT

PRINCIPAL

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II Year, I Semester, ECE-D, Class Time Table for the A.Y. 2020-21

Room No.: 3304 w.e.f: 17-08-2020

DAY	1	2		3	4		5	6	7
	9:10 to 10:00	10:00 to 10:50	10:50 to 11:00	11:00 to 11:50	11:50 to 12:40	12:40 to 1: 30	1:30 to 2:20	2:20 to 3:10	3:10 to 4:00
MON	DS	NMCV	BREAK	DS	IoT	LUNCH BREAK	EDC	S&S	NMCV
TUE	S&S	DS		IoT	NMCV		IOT LAB		
WED	IoT	S&S		EDC	DS		NMCV	EDC	QA&R
THU	EDC	DS		S&S	NMCV		S&S LAB		
FRI	NMCV	S&S		IoT	DS		EDC LAB		
SAT	EDC	QA&R		IoT	S&S		DS LAB		

NM&CV	: Numerical Methods & Complex Variables	Mr. D.Uma Shankar
EDC	: Electronic Devices & Circuits	Mr. B. Srinivasa Rao
S&S	: Signals& Systems	Mr. M. Srinivasa Rao
IoT	: Internet of Things	Sk. Zuber Basha
DS	: Data Structures	MsG.Prasanthi
EDC Lab	: Electronic Devices & Circuits Lab	Mr. T. Ravikanth Mr. B. Srinivasa Rao . Dr. Ayesha Dr. T. Santhi Mr.P.S.SChakravarthy Mr. A. Ravindra Babu Mr. P. Bhagya Raju Mr. N. Srinivasa Rao
S&S Lab	: Signals & Systems Lab	Dr. R. S. Siva Nayak Mr. M. Srinivasa Rao Ms.D.Sai Chandrika Dr.K.Laxma Reddy Dr. SK.SD. Basha
IoT Lab	: Internet of Things Lab	Dr.A.V.Nageswara Rao Ms.D.Sai Chandrika Mrs. J. Sravanthi Mr. Sk. Zuber Basha Dr.T.R.Chandra Babu
DS Lab	: Data Structures Lab	Ms. G.Prasanthi Mr. B.Sateesh Kumar

PRINCIPAL

SYLLABUS

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Subject Name& Code : Electronic Devices And Circuits (19BEC3TH02)
Regulation-R19

SYLLABUS

UNIT	DETAILS
I	**PN JUNCTION DIODE CHARACTERISTICS:** Insulators, Semiconductors and Metals–Classification using Energy gap, Intrinsic and Extrinsic Semiconductors. P-N Junction Diode - Formation of P-N Junction, Open Circuited P-N Junction, Biased P-N Junction - Forward Bias, Reverse Bias, Current Components in PN Junction Diode, Law of Junction, Diode Current Equation - Quantitative Analysis, V-I Characteristics of Diode - Forward Bias, Reverse Bias, Breakdown in P-N Junction Diode, Temperature Dependence on V-I Characteristics, Diode Resistance-Static Resistance, Dynamic Resistance, Reverse Resistance, Diode Capacitance - Transition Capacitance, Diffusion Capacitance, Energy Band Diagram of PN Junction Diode.
II	**SPECIAL DIODES AND RECTIFIERS:** Zener Diode - V-I Characteristics, Applications, Breakdown Mechanisms - Zener Breakdown and Avalanche Breakdown, Construction, Operation, Characteristics and applications of LED, LCD, Photodiode, Varactor Diode and Tunnel diode. **RECTIFIERS:** Basic Rectifier setup, Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Inductive and Capacitive Filters, L– Section and π- Section, Derive and compare rectifier parameters with and without filter.
III	**BIPOLAR JUNCTION TRANSISTOR (BJT):** Bipolar Junction Transistor – Types, Symbols and Operation, Transistor Current Components, Transistor Equation - Relation among IC, IB, ICBO, Transistor Configurations - CB, CE and CC, Transistor as a switch, Transistor switching times, Transistor as an Amplifier. Characteristics of Transistor in Common Base Configuration, Common Emitter and Common Collector Configurations - Input and output characteristics, Early effect, Transistor parameters, Current amplification factor, Relation among α, β, and γ, Comparison of CB, CE and CC Configurations, Punch Through/ Reach through, Typical transistor junction voltage values, Photo Transistor
IV	**BJT BIASING AND THERMAL STABILITY:** Need For Biasing, Operating Point, Load Line Analysis - D.C. Load Line, A.C. Load Line, Biasing - Methods, Basic Stability, Fixed Bias, Collector-to-base Bias and Self Bias, Stabilization against variations in VBE, Ic and β, Stability Factors S, S' and S'', Bias Compensation - Thermistor, Sensistor, Diode Compensation for variation in ICO, Thermal Runaway, Thermal Stability.
V	**FET & OTHER TRANSISTORS:** FET Types and Symbols - JFET and MOSFET/IGFET, JFET: N- Channel and P-Channel Construction, Operation, Characteristics - Drain and Transfer, Parameters - Drain Resistance, Amplification factor, Transconductance, Pinch-off voltage, MOSFET - Types - Depletion MOSFET - N Channel and P Channel, Enhancement MOSFET - N-Channel and P-Channel, Construction, Operation, Characteristics - Transfer and Drain Characteristics for Depletion and Enhancement Modes , Comparison between JFET and MOSFET.SCR-Symbol, Two-Transistor version, DIAC, TRIAC, UJT - Negative Resistance Property and Applications.

TEXT BOOKS	
T	**BOOK TITLE/AUTHORS/PUBLISHER**
T1	Electronic Devices and Circuits – J. Millman, C. Halkias, Tata McGraw-Hill, Third Edition, 2010.
T2	Electronic Devices and Circuits – Allen Mottershed, PHI, 2011.
T3	Electronic Devices and Circuits – Salivahanan, N. Suresh Kumar, A. Vallavaraj, Tata McGraw-Hill, Second Edition, 2008.
REFERENCE BOOKS	
R	**BOOK TITLE/AUTHORS/PUBLISHER**
R1	Integrated Electronics – Jacob Millman, C. Halkies, C.D. Parikh, Satyabrata Jit, Tata McGraw-Hill, Second Edition, 2011.
R2	Electronic Devices and Circuit Theory – R.L. Boylestad and Louis Nashelsky, Pearson Publications, Eleventh Edition, 2013.
R3	Electronic Devices and Circuits – A.P. Godse and U.A. Bakshi, Technical Publications, First Edition, 2009.

Lesson Plan

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Lesson Plan

Name of the Subject : Electronic Devices & Circuits **Class:** II B.Tech- I Sem

Name of the Staff:

Lecture No	Topic	Teaching Methodology	Hours Required	Reference Text Book
UNIT – I PN JUNCTION DIODE CHARACTERISTICS				
1	Insulators, Semiconductors and Metals–Classification using Energy gap	Chalk/Duster	1	T1,T3
2	Intrinsic and Extrinsic Semiconductors	Chalk/Duster	1	T1,T3
3	P-N Junction Diode - Formation of P-N Junction, Open Circuited P-N Junction	Chalk/Duster	1	T1,T3
4	Biased P-N Junction - Forward Bias, Reverse Bias	Chalk/Duster	1	T1,T3
5	Current Components in PN Junction Diode, Law of Junction	Chalk/Duster	1	T1,T3
6	Diode Current Equation - Quantitative Analysis	Chalk/Duster	1	T1,T3
7	V-I Characteristics of Diode - Forward Bias, Reverse Bias,	Chalk/Duster	1	T1,T3
8	Breakdown in P-N Junction Diode	Chalk/Duster	1	T1,T3
9	Temperature Dependence on V-I Characteristics, Diode Resistance-Static Resistance	Chalk/Duster	1	T1,T3
10	Dynamic Resistance, Reverse Resistance	Chalk/Duster	1	T1,T3
11	Diode Capacitance - Transition Capacitance, Diffusion Capacitance	Chalk/Duster	1	T1,T3
12	Energy Band Diagram of PN Junction Diode	Chalk/Duster	1	T1,T3
Total no. of hours required			**12**	
UNIT - II WATER TREATMENT AND WATER DISTRIBUTION				
13	Zener Diode - Construction, Operation	Chalk/Duster/PPT	1	T1,T3
14	Zener Diode - V-I Characteristics,Applications	Chalk/Duster/PPT	1	T1,T3
15	Breakdown Mechanisms - Zener Breakdown and Avalanche Breakdown	Chalk/Duster/PPT	1	T1,T3

16	Characteristics and applications of LED	Chalk/Duster	1	T1,T3
17	LCD,Photodiode	Chalk/Duster	1	T1,T3
18	Varactor Diode and Tunnel diode	Chalk/Duster	1	T1,T3
19	Basic Rectifier setup	Chalk/Duster	1	T1,T3
20	Half Wave Rectifier	Chalk/Duster	1	T1,T3
21	Full Wave Rectifier	Chalk/Duster	1	T1,T3
22	Bridge Rectifier	Chalk/Duster	1	T1,T3
23	Inductive and Capacitive Filters, L–Section and π- Section	Chalk/Duster	1	T1,T3
24	Derive and compare rectifier parameters with and without filter.	Chalk/Duster	1	T1,T3
	Total no. of hours required		**12**	
UNIT - III BIPOLAR JUNCTION TRANSISTOR (BJT)				
25	Bipolar Junction Transistor – Types, Symbols and Operation	Chalk/Duster	1	T1,T3
26	Transistor Current Components, Transistor Equation - Relation among I_C, I_B, I_{CBO}	Chalk/Duster	1	T1,T3
27	Transistor Configurations - CB	Chalk/Duster	1	T1,T3
28	Transistor Configurations - CE and CC	Chalk/Duster	1	T1,T3
29	Transistor as a switch, Transistor switching times	Chalk/Duster	1	T1,T3
30	Transistor as an Amplifier	Chalk/Duster	1	T1,T3
31	Characteristics of Transistor in Common Base Configuration-input and output	Chalk/Duster	1	T1,T3
32	Characteristics of Transistor in CB&CC Configurations-input and output	Chalk/Duster	1	T1,T3
33	Early effect, Transistor parameters	Chalk/Duster	1	T1,T3
34	amplification factor, Relation among α, β, and γ,	Chalk/Duster	1	T1,T3
35	Current Comparison of CB, CE and CC Configurations, Punch Through/ Reach through	Chalk/Duster	1	T1,T3
36	Typical transistor junction voltage values, Photo Transistor	Chalk/Duster	1	T1,T3
	Total no. of hours required		**12**	
UNIT - IV BJT BIASING AND THERMAL STABILITY				
37	Need For Biasing, Operating Point	Chalk/Duster	1	T1,T3
38	Load Line Analysis - D.C. Load Line	Chalk/Duster	1	T1,T3

39	A.C. Load Line	Chalk/Duster	1	T1,T3
40	Biasing - Methods, Basic Stability	Chalk/Duster	1	T1,T3
41	Fixed Bias	Chalk/Duster	1	T1,T3
42	Collector-to-base Bias	Chalk/Duster	1	T1,T3
43	Self Bias	Chalk/Duster	1	T1,T3
44	Stabilization against variations in VBE, Ic and β, Stability Factors S, S' and S''	Chalk/Duster	1	T1,T3
45	Bias Compensation - Thermistor	Chalk/Duster	1	T1,T3
46	Sensistor	Chalk/Duster	1	T1,T3
47	Diode Compensation for variation in ICO	Chalk/Duster	1	T1,T3
48	Thermal Runaway, Thermal Stability	Chalk/Duster	1	T1,T3
Total no. of hours required			**12**	
UNIT - V FET & OTHER TRANSISTORS:				
49	FET Types and Symbols - JFET and MOSFET/IGFET	Chalk/Duster/PPT	1	T1,T3
50	JFET: N- Channel - Construction, Operation	Chalk/Duster/PPT	1	T1,T3
51	JFET: P-Channel Construction, Operation	Chalk/Duster/PPT	1	T1,T3
52	Characteristics - Drain and Transfer	Chalk/Duster/PPT	1	T1,T3
53	Parameters - Drain Resistance, Amplification factor, Trans conductance, Pinch-off voltage	Chalk/Duster/PPT	1	T1,T3
54	Depletion MOSFET - N Channel – construction &operation	Chalk/Duster/PPT	1	T1,T3
55	Depletion MOSFET - P Channel-construction &operation	Chalk/Duster/PPT	1	T1,T3
56	Enhancement MOSFET - N-Channel and P-Channel-construction &operation	Chalk/Duster	1	T1,T3
57	Characteristics - Transfer and Drain Characteristics for Depletion and Enhancement Modes	Chalk/Duster	1	T1,T3
58	Analysis of MOSFETs, Comparison between JFET and MOSFET	Chalk/Duster	1	T1,T3
59	SCR- Symbol, Two-Transistor version	Chalk/Duster	1	T1,T3
60	UJT - Negative Resistance Property and Applications.	Chalk/Duster	1	T1,T3
Total no. of hours required			**12**	
GRAND TOTAL			**60**	

TEXT BOOKS	
T	**BOOK TITLE/AUTHORS/PUBLISHER**
T1	Electronic Devices and Circuits – J. Millman, C. Halkias, Tata McGraw-Hill, Third Edition, 2010.
T2	Electronic Devices and Circuits – Allen Mottershed, PHI, 2011.
T3	Electronic Devices and Circuits – Salivahanan, N. Suresh Kumar, A. Vallavaraj, Tata McGraw-Hill, Second Edition, 2008.
REFERENCE BOOKS	
R	**BOOK TITLE/AUTHORS/PUBLISHER**
R1	Integrated Electronics – Jacob Millman, C. Halkies, C.D. Parikh, Satyabrata Jit, Tata McGraw-Hill, Second Edition, 2011.
R2	Electronic Devices and Circuit Theory – R.L. Boylestad and Louis Nashelsky, Pearson Publications, Eleventh Edition, 2013.
R3	Electronic Devices and Circuits – A.P. Godse and U.A. Bakshi, Technical Publications, First Edition, 2009.

Signature of the Staff Member

HOD

HEAD OF THE DEPARTMENT
DEPT.OF ELECTRONICS AND COMMUNICATION ENGG.
NARASARAOPETA ENGINEERING COLLEGE
NARASARAOPET-522 601

CO-PO& PSO Mapping and assessment

NARASARAOPETA
NEC ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Name of the Subject : Electronic Devices And Circuits (19BEC3TH02)
Year/Sem :II/I **Regulation**-R19 **Academic Year**: 2020-21

CO Attainment					
CO	**CO Attainment Level (Mid)**	**CO Attainment Level (External)**	**Direct CO Attainment Level (Internal * 30%) + (External * 70%)**	**Indirect CO Attainment Level**	**Total CO Attainment Level (Direct CO Attainment * 90% + Indirect CO Attainment * 10%)**
C214.1	2	2	2	3	3
C214.2	1	0	1	3	2
C214.3	0	2	2	3	3
C214.4	1	0	1	3	2
C214.5	1	0	1	3	2
C214.6	3	0	1	3	2
C214.6					2.5

Signature of the Faculty Incharge

NARASARAOPETA
NEC ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Name of the Subject : Electronic Devices And Circuits (19BEC3TH02)
Year/Sem :II/I **Regulation**-R19 **Academic Year**: 2020-21

CO-PO MAPPING

CO-PO Mapping												
COs	POs											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
C214.1	1	1	1	1	-	-	-	-	-	-	-	-
C214.2	3	3	3	3	-	-	-	-	-	-	-	-
C214.3	3	2	2	2	-	-	-	-	-	-	-	-
C214.4	2	1	2	1	-	-	-	-	-	-	-	-
C214.5	2	3	2		-	-	-	-	-	-	-	-
C214.6	2		3		-	-	-	-	-	-	-	-
C214	2.16666667	2	2.166667	1.75	-	-	-	-	-	-	-	-

Total CO Attainment through Direct & Indirect Assessment	
CO Attainment	2.5

Signature of the Faculty Incharge

NARASARAOPETA
NEC ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Name of the Subject : Electronic Devices And Circuits (19BEC3TH02)
Year/Sem :II/I **Regulation**-R19 **Academic Year**: 2020-21

CO-PSO Mapping & PSO Attainment			
COs	PSOs		
	PSO1	PSO2	PSO3
C214.1	1	-	2
C214.2	1	-	2
C214.3	2	-	1
C214.4	1	-	2
C214.5	2	-	1
C214.6		-	2
C214	1.25	-	1.75
Total CO Attainment through Direct & Indirect Assessment			
CO Attainment			2.5
PSO Attainment			
COs	PSOs		
	PSO1	PSO2	PSO3
PSO Attainment	1.041666667	-	1.458333333

Signature of the Faculty Incharge

CO ATTAINMENT

NARASARAOPETA
NEC ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Name of the Subject : Electronic Devices And Circuits (19BEC3TH02)
Year/Sem :II/I **Regulation**-R19 **Academic Year**: 2020-21

PO-ATTAINMENT

CO-PO Mapping												
COs	POs											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
C214.1	1	1	1	1	-	-	-	-	-	-	-	-
C214.2	3	3	3	3	-	-	-	-	-	-	-	-
C214.3	3	2	2	2	-	-	-	-	-	-	-	-
C214.4	2	1	2	1	-	-	-	-	-	-	-	-
C214.5	2	3	2		-	-	-	-	-	-	-	-
C214.6	2		3		-	-	-	-	-	-	-	-
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Total CO Attainment through Direct & Indirect Assessment	
CO Attainment	2.5

PO Attainment												
	PO1	PO2	PO3	PO4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
PO Attainment	1.80555556	1.66667	1.805556	1.45833333	-	-	-	-	-	-	-	-

Signature of the Faculty Incharge

Web references

&

other pedagogical initiates details

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Year/Sem: II B.TECH I SEMESTER **Academic Year:** 2020-21

Course Name & Code: ELECTRONIC DEVICES AND CIRCUITS & 19BEC3TH02

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Student's Roll list

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Academic Year : 2020-21 **Year/Sem: II/I**

ROLL LIST

S.NO	H.T.NO	NAME OF THE STUDENT
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2	19471A0402	ALAKUNTA RAMESH
3	19471A0403	AURANGABAD MAHESH GOPI
4	19471A0404	BATCHU MAHESH
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6	19471A0406	CHERUKURI NIKHITHESWARI
7	19471A0407	CHERUKURI SRINIVASA RAO
8	19471A0408	CHEVURI AMARESWARI
9	19471A0409	CHIRAMPALLI YUVA SAI
10	19471A0410	CHITTA TEJA SRI
11	19471A0411	DINDU LOKESH
12	19471A0412	DUGGEMPUDI SRI BHAKTHANJANEYA
13	19471A0413	EMANI GAYATHRI
14	19471A0414	GADE RAJYALAKSHMI
15	19471A0415	GADIPARTHI KAVITHA
16	19471A0416	GANTA ASHOK REDDY
17	19471A0417	GOTTAM HARSHAVARDHAN REDDY
18	19471A0418	GUDDETI VENKATESWARLU
19	19471A0419	GUDIPATI ASHOK KUMAR
20	19471A0420	GUDIPUDI GOPI
21	19471A0421	GUNTURU VIJAYALAKSHMI
22	19471A0422	KOMMANABOYINA VENKATESWARLU
23	19471A0423	KONDAVANDLA CHANDU
24	19471A0424	KONDAVETI JAHNAVI
25	19471A0425	KONDEBOINA LAKSHMI NARAYANA
26	19471A0426	KONDEDDULA SWATHI
27	19471A0429	MADDULA VENKATESWARLU
28	19471A0430	MAILA TIRUPATHI
29	19471A0431	MANDAPATI TIRUPATHI RAO
30	19471A0432	MARLAPATI KIRAN KUMAR
31	19471A0433	MARTHALA SAI SWETHA
32	19471A0434	MARURI PRIYANKA
33	19471A0435	NANDALA PRAVEEN
34	19471A0436	NOOKALA NAVEEN KUMAR
35	19471A0437	ORCHU SAI SIVA SATHVIKA

36	19471A0438	PAMARTHI VENKATA SUBRAHMANYA CHARI
37	19471A0439	PANGULURI SRI MANI DEEP
38	19471A0440	PONDUGULA BHARGAV REDDY
39	19471A0441	PUPPALA VENKATA SIVA SAI GOPICHAND
40	19471A0442	SANNEBOINA VENKATA HARI
41	19471A0443	SHAIK ARSHAD ALI
42	19471A0444	SHAIK MABU SUBHANI
43	19471A0445	SHAIK MOHAMMAD ALI
44	19471A0446	SHAIK MOHAMMAD RAFFI
45	19471A0447	SHAIK SAIDU BABU
46	19471A0448	SHAIK SHAZIAH BANU
47	19471A0449	SIKHINAM VENKATA RAMANJANEYULU
48	19471A0450	SINGAMREDDY AMARNADH REDDY
49	19471A0451	SINKA GOWRI SANKAR SRINIVAS
50	19471A0452	SOMISETTY MADHU RAMYA SAI
51	19471A0453	SUNKARA SRI LAKSHMI TULASI
52	19471A0454	TANIPARTHI HARICHANDANA
53	19471A0455	THOKALA TWINKLE
54	19471A0456	TULAVA GOPI
55	19471A0457	VALLEM ESWARSAI KUMAR
56	19471A0458	VANGAVOLU DEEPTHI
57	19471A0459	VARRA HARINI REDDY
58	19471A0460	YAMPARALA GOPI
59	19471A0461	AKASH REDDY BADE
60	19471A0462	ANNAPUREDDY PARAMESWARA REDDY
61	19471A0463	APPANABOINA GOPI KRISHNA
62	19471A0464	ARAVAPALLI HITESH LAKSHMAN KUMAR
63	19471A0465	ATMAKURI RAMASAI
64	19471A0466	BADDEPOGU RAMYA
65	19471A0467	BALLARI SWARUP KUMAR
66	19471A0468	BEERAM ANUSHA
67	19471A0469	BEJJANKI HARI PRASAD
68	19471A0470	BELLAMKONDA ARUN KUMAR
69	19471A0471	CHEVULA JAYASRI
70	19471A0472	DARA VISHNUVARDHAN
71	19471A0473	DIVVELA BALA LAKSHAMANA SADA SIVA
72	19471A0474	GADE HARIKA
73	19471A0475	GATTUPALLI SAI SASANK
74	19471A0476	GONUGUNTLA VYSHNAVI
75	19471A0477	GOSULA AMARA BHARGAVI
76	19471A0478	GUDI REVANTH KUMAR
77	19471A0479	GUTTIKONDA TANUJA
78	19471A0480	JAGARLAMUDI SAI POOJA
79	19471A0481	KAMEPALLI SRI VENKATA JAYA KRISHNA
80	19471A0482	KARNATI MANI GOPINADH
81	19471A0483	KATURI KISHORE
82	19471A0484	KOMIRI ANAND BABU

83	19471A0485	KONDAPALLI SIVADURGA
84	19471A0486	MARAMREDDY RAKESH REDDY
85	19471A0487	MEKALA LAKSHMI
86	19471A0488	MEKAPOTHULA SRINADH
87	19471A0489	MUDIYALA NITHIN REDDY
88	19471A0490	MUNNA NARENDRA
89	19471A0491	MUNNANGI UMA MAHESWARA REDDY
90	19471A0492	MUTUKURI ARUN KUMAR
91	19471A0493	NALLAGORLA GOPI
92	19471A0495	NIMMAKAYALA NAVEEN
93	19471A0496	PALAPARTHI PHANINDRA
94	19471A0497	PENDYALA MAHESH KUMAR
95	19471A0498	POTHABATHINI NAGA SARATH KUMAR
96	19471A0499	POTLA VENEELA
97	19471A04A0	RAJA RAJYALAKSHMI AKSHAYA
98	19471A04A1	RAJARAPU SAMPADA
99	19471A04A2	RAKESH YAMPARALA
100	19471A04A3	SAMPATHI SRIKANTH
101	19471A04A4	SHAIK ABDUL RAHAMAN
102	19471A04A5	SHAIK AMANULLA
103	19471A04A6	SHAIK INAMUL HUSSEN
104	19471A04A7	SHAIK KHATIB MAHAMMAD ABBAS
105	19471A04A8	SHAIK MUSARATH FARHANA
106	19471A04A9	SHAIK SAMEER BASHA
107	19471A04B0	SHAIK TANVEER SUHEERA
108	19471A04B1	SYED HUSSAINBI
109	19471A04B2	TAMMISETTY NITISH KUMAR
110	19471A04B3	THOTA SAI TEJA
111	19471A04B4	VAMSI KRISHNA BIKKI
112	19471A04B5	VEJENDLA MAHESH GOPAL
113	19471A04B6	VEMULURI HEMANTH
114	19471A04B7	VENKATA SANDHYA SYAMALA
115	19471A04B8	VUYYURU REVANTH
116	19471A04B9	YARAGALLA JAYAKANTH
117	19471A04C0	YARRAMREDDY JAYA SRI
118	19471A04C1	ACHANALA GOPINATH
119	19471A04C2	ADURI AMULYA
120	19471A04C3	AMBATI SUBRAMANYAM
121	19471A04C4	ANNA RAKESH
122	19471A04C5	ARIGELA KRISHNA BALAJI
123	19471A04C6	ATTHOTA MANI KUMAR
124	19471A04C7	BALUSUPATI CHIRANJEEVI
125	19471A04C8	BANDI PRIYANKA
126	19471A04C9	BODDULURI YOGA ALEKHYA
127	19471A04D0	BURRI VENKATA NAGA GOPI
128	19471A04D1	BUSA GNANESWAR
129	19471A04D2	CH MANI KUMAR

130	19471A04D3	CHINTHALACHERUVU VENKATESH
131	19471A04D4	CHUKKA ANOOP
132	19471A04D5	DERANGULA VIJAYA BHASKAR
133	19471A04D6	DEVANABOINA HEMANTH
134	19471A04D7	DODDA SRI VENKATA GOPAL REDDY
135	19471A04D8	GAJJALA UJWALA
136	19471A04D9	GARNEPUDI SUMANTH
137	19471A04E0	GUDIBANDLA SIVA RAMA KRISHNA REDDY
138	19471A04E1	GULLA VAMSI
139	19471A04E2	JADDA YEDUKONDALU
140	19471A04E3	JAJULA SIVA TEJA
141	19471A04E4	JALLI JOHN SAMUEL
142	19471A04E5	JAMMOJU VENU GOPALACHARI
143	19471A04E6	JUPUDI AJAY KUMAR
144	19471A04E7	KANKANALA DEVI AJAY SRINIVAS
145	19471A04E8	KARUMANCHI SAI KIRAN
146	19471A04E9	KASARAGADDA JAGADEESH
147	19471A04F0	KESANAPALLI JYOTHIRMAI
148	19471A04F1	KOKKERA PAVAN KUMAR
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153	19471A04F7	KOYYA APARNA
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172	19471A04H6	SHAIK SAMEER
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174	19471A04H8	SURE ESWAR PRASAD
175	19471A04H9	VAJRALA GOUTHAMI
176	19471A04I0	VAJRALA NAVEENA

177	19471A04I1	AASAM VIJAYA LAKSHMI
178	19471A04I2	ALLA MASTAN RAO
179	19471A04I3	ANJANEYULU DEVARASETTY
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213	19471A04L7	S SHARIQA
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216	19471A04M0	SHAIK KHALEEL REHAMAN
217	19471A04M1	SHAIK MASTAN SHARIEF
218	19471A04M2	SHAIK NAGOOR MEERAVALI
219	19471A04M3	SHAIK SADHIK ALLABHAKSHU
220	19471A04M4	SONTI DEEPAK KUMAR
221	19471A04M5	UDALA NAGESWAR RAO
222	19471A04M6	VADRA JYOTHI
223	19471A04M7	VAKA NARENDRA KUMAR

224	19471A04M8	YADALA CHANDRA MAHESH REDDY
225	19471A04M9	YAKKALA ASHA
226	19471A04N0	THINNALURI BINDU MADHAV
227	19471A04N1	KONGA BRAHMA TEJA
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232	18471A0462	ANNAM VAMSI KRISHNA
233	18471A04M0	VIPPARLA ARUN KUMAR
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244	20475A0411	KOCHARLA RAMYA
245	20475A0412	DULAM HARSHAVARDHAN
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248	20475A0415	PAYARDHA SAGAR BABU
249	20475A0416	YAKKALA YOGA LAKSHMI
250	20475A0417	DHARANI DEVI GARIKAPATI
251	20475A0418	ANDE SIREESHA
252	20475A0419	TIRUMALASETTI NIHARIKA
253	20475A0420	NAMPALLI AMRUTHA
254	20475A0421	SANGAM HENA GRACE
255	20475A0422	BOLLISETTY LEELA SRINIVASA KUMAR
256	20475A0423	NAGINENI NARENDRA
257	20475A0424	BANDARU VAMSI KRISHNA
258	20475A0425	VALAJIPETA DEVA KRISHNA SUMANTH
259	20475A0426	THATIKOLA GANESH

HOD,ECE

Hand Written / Printed Lecture Notes / Material given to the Students

CHAPTER-I

PN JUNCTION DIODE CHARACTERISTICS

Insulators, Semiconductors and Metals–Classification using Energy gap, Intrinsic and Extrinsic Semiconductors. P-N Junction Diode - Formation of P-N Junction, Open Circuited P-N Junction, Biased P-N Junction - Forward Bias, Reverse Bias, Current Components in PN Junction Diode, Law of Junction, Diode Current Equation - Quantitative Analysis, V-I Characteristics of Diode - Forward Bias, Reverse Bias, Breakdown in P-N Junction Diode, Temperature Dependence on V-I Characteristics, Diode Resistance-Static Resistance, Dynamic Resistance, Reverse Resistance, Diode Capacitance - Transition Capacitance, Diffusion Capacitance, Energy Band Diagram of PN Junction Diode.

1. OBJECTIVES

- To know the band theory of Semiconductors.
- Properties of various semi-conductors.
- Parameters of PN junction diode to be discussed.
- To study the basic operation and principles of PN diode.
- Applications of PN diodes are discussed.

1.1 INTODUCTION

Electronics: Electron + Mechanics

Electronics Engineering is a branch of engineering which deals with the flow of electrons in vacuum tubes,gas and semiconductor.

Devices: We are having the devices like function generator, Cathod Ray Oscilloscope (CRO), power supplies etc.

Circuit: The proper arrangement of the components like resistors, inductors, capacitors etc.

Applications of Electronics:

Home Appliances, Medical Applications, Robotics, Mobile Communication, Computer Communication etc.

1.2REVIEW OF THE SEMICONDUCTOR PHYSICS

1.2.1Atomic Structure

Atom is the basic building block of all the elements. It consists of the central nucleus of positive charge around which small negatively charged particles called electrons revolve in different paths or orbits. An Electrostatic force of attraction between electrons and the nucleus holds up electrons in differentorbits.

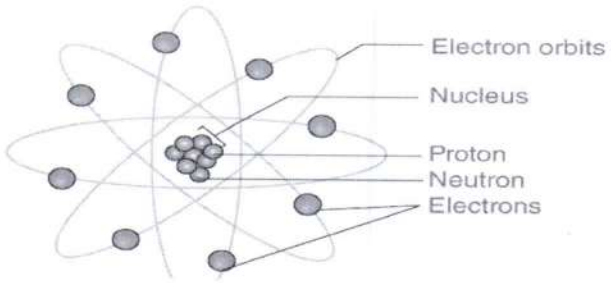

Figure 1.1: Atomic structure

Nucleus is the central part of an atom and contains protons and neutrons. A proton is positively charged particle, while the neutron has the same mass as the proton, but has no charge. Therefore, nucleus of an atom is positively charged.

atomic weight = no. of protons + no. of neutrons

An electron is a negatively charged particle having negligible mass. The charge on an electron is equal but opposite to that on a proton. Also, the number of electrons is equal to the number of protonsin an atom under ordinary conditions. Therefore, an atom is neutral as a whole.

atomic number = no. of protons or electrons in an atom

The number of electrons in any orbit is given by $2n^2$ where n is the number of the orbit.For example,

I orbit contains $2x1^2$ =2 electrons

II orbit contains $2x2^2$ = 8 electrons

III orbit contains $2x3^2$ = 18 electrons and so on

The last orbit cannot have more than 8 electrons.

The last but one orbit cannot have more than 18 electrons.

1.2.2 Positive and negative ions:

Protons and electrons are equal in number hence if an atom loses an electron, it has lost negative charge therefore it becomes positively charged and is referred as positive ion. If an atom gains an electron, it becomes negatively charged and is referred to as negative ion.

1.2.3 Valence electrons:

The electrons in the outermost orbit of an atom are known as valence electrons. The outermost orbit can have a maximum of 8 electrons. The valence electrons determine the physical and chemical properties of a material. When the number of valence electrons of an atom is less than 4, the material is usually a metal and a conductor. Examples are sodium, magnesium and aluminum, which have 1,2 and 3 valence electrons respectively.

When the number of valence electrons of an atom is more than 4, the material is usually a non-metal and an insulator. Examples are nitrogen, Sulphur and neon, which have 5,6 and 8 valence electrons respectively. When the number of valence electrons of an atom is 4 the material has both metal and non-metal properties and is usually a semi-conductor. Examples are carbon, silicon and germanium.

1.2.4 Free electrons:

The valence electrons of different material possess different energies. The greater the energy of a valence electron, the lesser it is bound to the nucleus. In certain substances, particularly metals, the valence electrons possess so much energy that they are very loosely attached to the nucleus. The loosely attached valence electrons move at random within the material and are called free electrons. The valence electrons, which are loosely attached to the nucleus, are known as free electrons.

1.2.5 Energy bands:

In case of a single isolated atom an electron in any orbit has definite energy. When atoms are brought together as in solids, an atom is influenced by the forces from other atoms. Hence an electron in any orbit can have a range of energies rather than single energy. These range of energy levels are known as Energy bands. Within any material there are two distinct energy bands in which electrons may exist viz, Valenceband and conduction band.

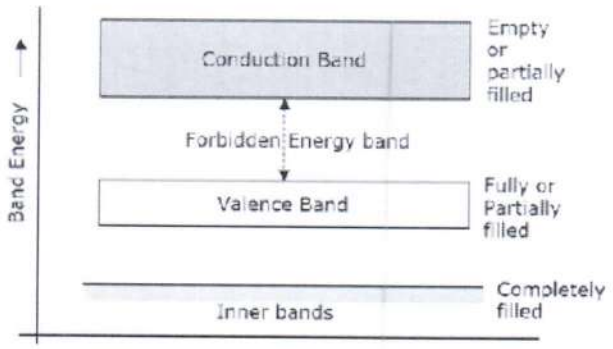

Figure 1.2: Energy level diagram

- The range of energies possessed by valence electrons is called valence band.
- The range of energies possessed by free electrons is called conduction band.
- Valence band and conduction band are separated by an energy gap in which no electrons normally exist this gap is called forbidden gap.

1.3 CLASSIFICATION OF MATERIALS BASED ON ENERGY BAND THEORY

Based on the width of the forbidden gap, materials are broadly classified as

- Conductors
- Insulators
- Semiconductors.

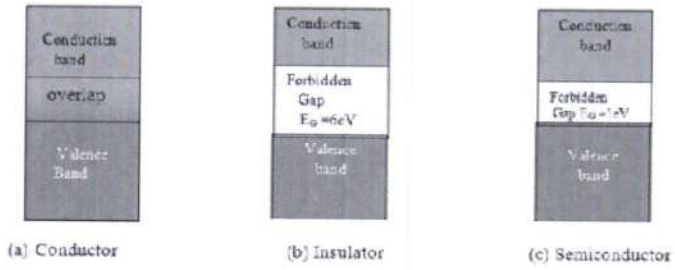

Figure 1.3: Classification of Materials

1.3.1 Conductors:

Conductors are those substances, which allow electric current to pass through them. Example: Copper, Al, salt solutions, etc. In terms of energy bands, conductors are those substances in

which there is no forbidden gap. Valence and conduction band overlap as shown in fig 1.3 (a). For this reason, very large number of electrons are available for conduction even at extremely low temperatures. Thus, conduction is possible even by a very weak electric field.

1.3.2 Insulators:

Insulators are those substances, which do not allow electric current to pass through them. Example: Rubber, glass, wood etc. In terms of energy bands, insulators are those substances in which the forbidden gap is very large. Thus, valence and conduction band are widely separated as shown in fig 1.3 (b). Therefore, insulators do not conduct electricity even with the application of a large electric field or by heating or at very high temperatures.

1.3.3 Semiconductors:

Semiconductors are those substances whose conductivity lies in between that of a conductor and Insulator. Example: Silicon, germanium, Cealenium, Gallium, arsenide etc. In terms of energy bands, semiconductors are those substances in which the forbidden gap is narrow. Thus, valence and conduction bands are moderately separated as shown in fig 1.3 (C). In semiconductors, the valence band is partially filled, the conduction band is also partially filled, and the energy gap between conduction band and valence band is narrow.

Therefore, comparatively smaller electric field is required to push the electrons from valence band to conduction band. At low temperatures the valence band is completely filled and conduction band is completely empty. Therefore, at very low temperature a semi-conductor actually behaves as an insulator.

1.4CLASSIFICATION OF SEMICONDUCTORS

Semiconductors are classified into two types.

(a) Intrinsic semiconductors.

(b) Extrinsic semiconductors.

a) Intrinsic semiconductors:

A semiconductor in an extremely pure form is known as Intrinsic semiconductor. Example: Silicon, germanium. Both silicon and Germanium are tetravalent (having 4 valence electrons). Each atom forms a covalent bond or electron pair bond with the electrons of neighboring atom. The structure is shown below.

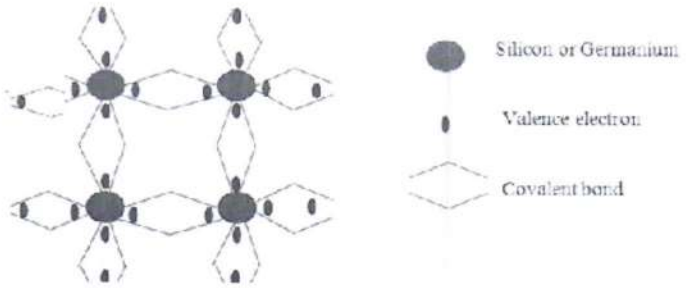

Figure 1.4: Crystalline structure of Silicon (or Germanium)

At Low Temperature

At low temperature, all the valence electrons are tightly bounded the nucleus hence no free electrons are available for conduction. The semiconductor therefore behaves as an Insulator at absolute zero temperature.

At room temperature

At room temperature, some of the valence electrons gain enough thermal energy to break up the covalent bonds. This breaking up of covalent bonds sets the electrons free and is available for conduction.

When an electron escapes from a covalent bond and becomes free electrons, a vacancy is created in a covalent bond as shown in figure above. Such a vacancy is called Hole. It carries positive charge and moves under the influence of an electric field in the direction of the electric field applied. Numbers of holes are equal to the number of electrons since; a hole is nothing but an absence of electrons.

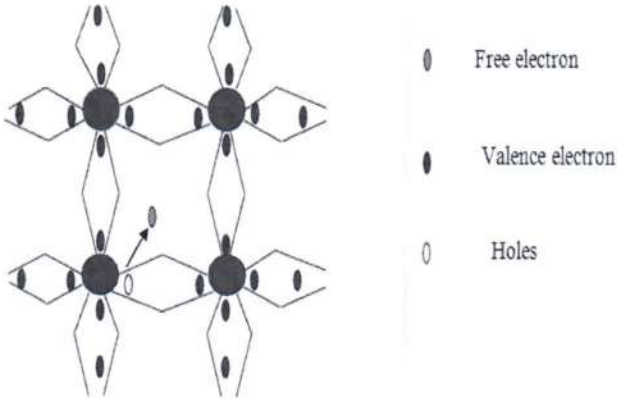

Figure 1.5: Crystalline structure of Silicon (or Germanium) at room temperature

b) Extrinsic Semiconductor:

When an impurity is added to an intrinsic semiconductor its conductivity changes. This, process of adding impurity to a semiconductor is called Doping and the impure semiconductor is called extrinsic semiconductor. Depending on the type of impurity added, extrinsic semiconductors are further classified as n-type and p-type semiconductor.

1.4.1 N-type semiconductor:

When a small amount of Pentavalent impurity is added to a pure semiconductor it is called as n-type semiconductor. Addition of Pentavalent impurity provides a large number of free electrons in a semiconductor crystal. Typical example for pentavalent impurities are Arsenic, Antimony and Phosphorus etc. Such impurities which produce n-type semiconductors are known as Donor impurities because they donateor provide free electrons to the semiconductor crystal. To understand the formation of n-type semiconductor, consider a pure silicon crystal with an impurity say arsenic added to it as shown in figure 1.6.

We know that a silicon atom has 4 valence electrons and Arsenic has 5 valence electrons. When Arsenic is added as impurity to silicon, the 4 valence electrons of silicon make co-valent bond with 4 valence electrons of Arsenic. The 5^{th} Valence electrons finds no place in the covalent bond thus, it becomes free and travels to the conduction band as shown in figure. Therefore, for each arsenic atom added, one free electron will be available in the silicon crystal. Though each arsenic atom provides one free electron yet an extremely small amount of arsenic impurity provides enough atoms to supply millions of free electrons. Due to thermal energy, still hole election pairs are generated but the number of free electrons are very large in number when compared to holes. So in an n-type semiconductor electrons are majority charge carriers and holes are minority charge carriers. Since the current conduction is pre-dominantly by free electrons (- vely charges) it is called as n-type semiconductor(n- means –ve).

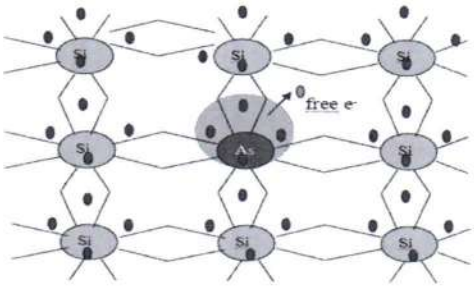

Figure 1.6: N-type semiconductor

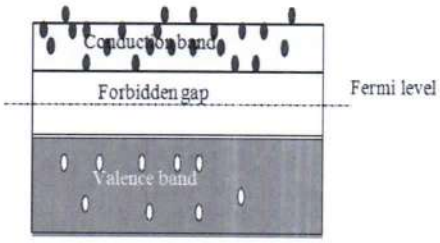

Figure 1.7: Energy band diagram for n-type semiconductor

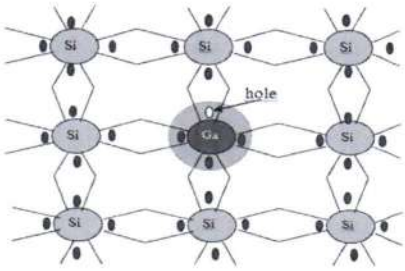

Figure 1.8: P-type semiconductor

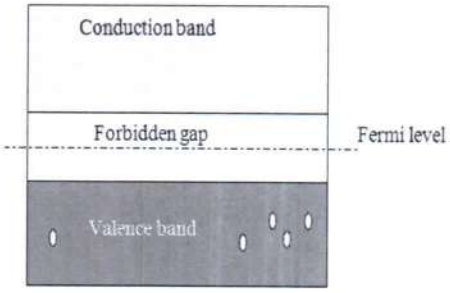

Figure 1.9: Energy band diagram for

1.4.2 P-type semiconductor:

When a small amount of trivalent impurity is added to a pure semiconductor it is called p-type semiconductor. The addition of trivalent impurity provides large number of holes in the semiconductor crystals. Example: Gallium, Indium or Boron etc. Such impurities which produce p-type semiconductors are known as acceptor impurities because the holes created can accept the electrons in the semi- conductor crystal. To understand the formation of p-type semiconductor, consider a pure silicon crystal with an impurity say gallium added to it as shown in figure 8.

We know that silicon atom has 4 valence electrons and Gallium has 3 electrons. When Gallium is added as impurity to silicon, the 3 valence electrons of gallium make 3 covalent bonds with 3 valenceelectrons of silicon. The 4^{th} valence electrons of silicon cannot make a covalent bond with that of Gallium because of short of one electron as shown above. This absence of electron is called a hole. Therefore, for each gallium atom added one hole is created, a small amount of Gallium provides millions of holes.

Due to thermal energy, still hole-electron pairs are generated but the number of holes is very large compared to the number of electrons. Therefore, in a p-type semiconductor holes are majority carriers and electrons areminority carriers. Since the current conduction is predominantly by hole (+ charges) it is called as p-type semiconductor (p means +ve).

1.5 Electrons and Holes

1.5.1 Conduction in solids:

Conduction in any given material occurs when a voltage of suitable magnitude is applied to it, whichcauses the charge carriers within the material to move in a desired direction.This may be due to electron motion or hole transfer or both.

1.5.2 Electron motion:

Free electrons in the conduction band are moved under the influence of the applied electric field. Since electrons have negative charge, they are repelled by the negative terminal of the applied voltage and attracted towards the positive terminal.

1.5.3 Hole transfer:

Hole transfer involves the movement of holes. Holes may be thought of positive charged particles and as such they move through an electric field ina direction opposite to that of electrons.

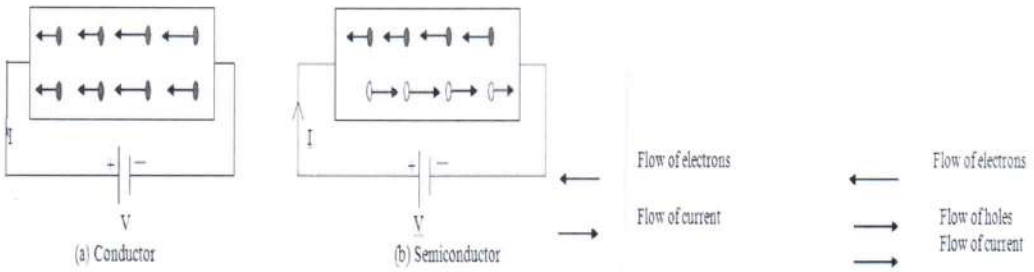

Figure 1.10: Flow of Electrons and Holes in Conductor and Semiconductor

In a good conductor (metal) as shown in fig (a) the current flow is due to free electrons only. In a semiconductor as shown in fig (b). The current flow is due to both holes and electrons moving in opposite directions. The unit of electric current is Ampere (A) and since the flow of electric current is constituted by the movement of electrons in conduction band and holes in valence band, electrons and holes are referred as charge carriers.

1.6 P-N Junction Diode

When a p-type semiconductor material is suitably joined to n-type semiconductor the contactsurface is called a p-n junction. The p-n junction is also called as semiconductor diode.

1.6.1 Applications of diode:

a. Used as rectifier diodes in DC power suppliers
b. Used as clippers and clampers
c. Used as switch in logic circuit in computers
d. Used as voltage multipliers.

1.6.2 Construction and working of a PN Junction diode:Open Circuited PN Junction:

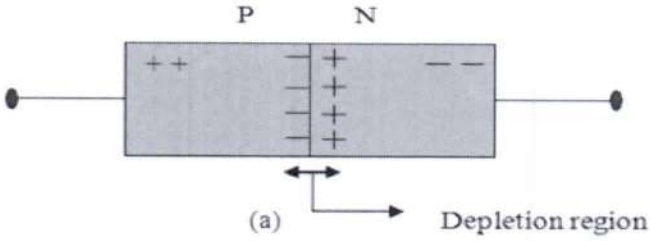

Figure 1.11 (a): PN Junction

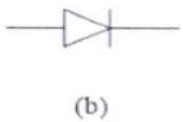

Figure 1.11 (b): Symbol of PN Diode

The left side material is a p-type semiconductor having –ve acceptor ions and +vely charged holes. The right-side material is n-type semiconductor having +ve donor ions and free electrons. Suppose the two pieces are suitably treated to form pn junction, then there is a tendency for the free electrons from n-type to diffuse over to the p-side and holes from p-type to the n-side. This process is called diffusion.

As the free electrons move across the junction from n-type to p-type, +ve donor ions are uncovered. Hence a +ve charge is built on the n-side of the junction. At the same time, the free electrons cross the junction and uncover the –ve acceptor ions by filling in the holes. Therefore, a net –ve charge is established on p-side of the junction. When a sufficient number of donor and acceptor ions is uncovered further diffusion is prevented. Thus, a barrier is set up against further movement of charge carriers. This is called potential barrier orjunction barrier Vo. The potential barrier is of the order of 0.1 to 0.3V.

Note: outside this barrier on each side of the junction, the material is still neutral. Only inside the barrier,there is a +ve charge on n-side and –ve charge on p-side. This region is called depletion layer.

1.6.3 Biasing of a PN junction diode:

Connecting a p-n junction to an external DC voltage source is called biasing.

i. Forward biasing

ii. Reverse biasing

i. Forward biasing

When external voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow is called forward biasing. To apply forward bias, connect +ve terminal of the battery to p-type and –ve terminal to n-type as shown in fig.1.12 below. The applied forward potential (V_F) establishes the electric field which acts against the field due to potential barrier. Therefore, the resultant field is weakened and the barrier height is reduced at the junction as shown in fig. 1.12. Since the potential barrier voltage is very small, a small forward voltage (V_F) is sufficient to completely eliminate the barrier. Once the potential barrier is eliminated by the forward voltage, junction resistance (R_F) becomes almost zero and a low resistance path is established for the entire circuit. Therefore, current flows in the circuit. This is called forward current (I_F).

CHAPTER-II

SPECIAL DIODES AND RECTIFIERS

Content:

Special Diodes: Zener Diode – V-I characteristics, Applications, Breakdown Mechanisms-Zener Breakdown and Avalanche Breakdown, Construction, Operation, Characteristics and applications of LED, LCD, Photodiode, Varactor Diode and Tunnel diode.

Rectifiers: Basic Rectifier setup, Half wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Inductive and Capacitive Filters, L-Section (CLC filter) and P-section, Rectifier parameters with and without filters.

2. OBJECTIVES

- After the completion of this chapter, we should able to understand:
- To know the operation of Special Diodes.
- Applications of Special Diodes in various electronic circuits are discussed.
- To know the operation of rectifiers and Application.
- Construct and analyse the both half wave and full wave rectifiers with and without filters.

2.1 SPECIAL DIODES

2.1.1 Zener Diode:

A Zener diode is a heavily doped semiconductor device that is designed to operate in the reverse direction. The Zener diode is like a general-purpose signal diode consisting of a silicon PN junction. When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but as soon as a reverse voltage applied across the zener diode exceeds the rated voltage of the device, the diodes breakdown voltage VB is reached at which point a process called Avalanche Breakdown occurs in the semiconductor depletion layer and a current

starts to flow through the diode to limit this increase in voltage.

The current now flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor) and once achieved this reverse saturation current remains fairly constant over a wide range of applied voltages. This breakdown voltage point, VB is called the "zener voltage" for zener diodes and can range from less than one volt to hundreds of volts.

The point at which the zener voltage triggers the current to flow through the diode can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes semiconductor construction giving the diode a specific zener breakdown voltage, (Vz) for example, 4.3V or 7.5V. This zener breakdown voltage on the I-V curve is almost a vertical straight line.

2.1.2 Zener Diode I-V Characteristics

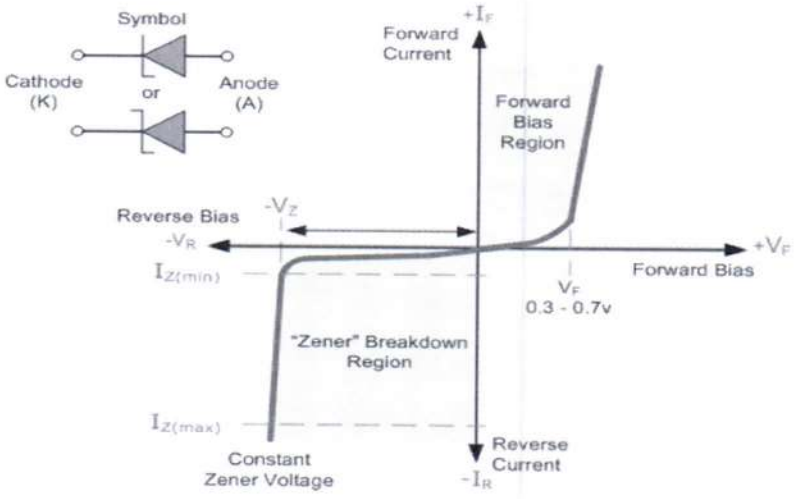

Figure 2.1: V-I Characteristics of Zener Diode and Symbol

The Zener Diode is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply. From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly

constant even with large changes in current as long as the zener diodes current remains between the breakdown current IZ (min)and the maximum current rating IZ (max).

This ability to control itself can be used to great effect to regulate or stabilize a voltage source against supply or load variations. The fact that the voltage across the diode in the breakdown region is almost constant turns out to be an important application of the zener diode as a voltage regulator. The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum IZ (min)value in the reverse breakdown region.

2.1.3 Applications of Zener Diode

- As a voltage regulator.
- Protects from over voltage.
- Used in clipping circuits.
- Used to shift voltage.

2.1.4 Breakdown Mechanisms- Zener Breakdown and Avalanche Breakdown

i) Avalanche breakdown:

Avalanche breakdown occurs both in normal diode and Zener Diode at high reverse voltage. When a high value of reverse voltage is applied to the PN junction, the free electrons gain sufficient energy and accelerate at high velocities. These free electrons moving at high velocity collides other atoms and knocks off more electrons. Due to this continuous collision, a large number of free electrons are generated as a result of electric current in the diode rapidly increases. This sudden increase in electric current may permanently destroy the normal diode, however, a Zener diode is designed to operate under avalanche breakdown and can sustain the sudden spike of current. Avalanche breakdown occurs in Zener diodes with Zener voltage (Vz) greater than 6V.

ii) Zener Breakdown in Zener Diode

When the applied reverse bias voltage reaches closer to the Zener voltage, the electric field in the depletion region gets strong enough to pull electrons from their valence band. The valence electrons that gain sufficient energy from the strong electric field of the depletion region break free from the parent atom. At the Zener breakdown region, a small increase in the voltage results in the rapid increase of the electric current.

2.2 LED (Light Emitting Diode):

Light Emitting Diodes or LED's, are among the most widely used of all the different types of semiconductor diodes available today and are commonly used in TV's and colour displays. They are the most visible type of diode, that emit a fairly narrow bandwidth of either visible light at different coloured wavelengths, invisible infra-red light for remote controls or laser type light when a forward current is passed through them.

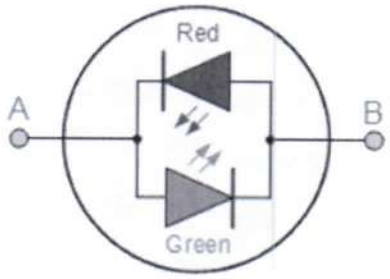

Figure 2.2: The Light Emitting Diode

The "Light Emitting Diode" or as it is more commonly called, is basically just a specialised type of diode as they have very similar electrical characteristics to a PN junction diode. This means that an LED will pass current in its forward direction but block the flow of current in the reverse direction. Related Products: LEDs and LED Lighting Optical Lenses

Light emitting diodes are made from a very thin layer of fairly heavily doped semiconductor material and depending on the semiconductor material used and the amount of

doping, when forward biased an LED will emit a coloured light at a particular spectral wavelength. When the diode is forward biased, electrons from the semi-conductors conduction band recombine with holes from the valence band releasing sufficient energy to produce photons which emit a monochromatic (single colour) of light. Because of this thin layer a reasonable number of these photons can leave the junction and radiate away producing a coloured light output.

Figure 2.3: LED Construction

Then we can say that when operated in a forward biased direction Light Emitting Diodes are semiconductor devices that convert electrical energy into light energy. The construction of a Light Emitting Diode is very different from that of a normal signal diode. The PN junction of an LED is surrounded by a transparent, hard plastic epoxy resin hemispherical shaped shell or body which protects the LED from both vibration and shock. Surprisingly, an LED junction does not actually emit that much light, so the epoxy resin body is constructed in such a way that the photons of light emitted by the junction are reflected away from the surrounding substrate base to which the diode is attached and are focused upwards through the domed top of the LED, which itself acts like a lens concentrating the amount of light. Therefore, the emitted light appears to be brightest at the top of the LED.

However, not all LEDs are made with a hemispherical shaped dome for their epoxy shell. Some indication LEDs have a rectangular or cylindrical shaped construction that has a flat surface on top or their body is shaped into a bar or arrow. Generally, all LED's are manufactured with two legs protruding from the bottom of the body.

Also, nearly all modern light emitting diodes have their cathode, (–) terminal identified by either a notch or flat spot on the body or by the cathode lead being shorter than the other as the anode (+) lead is longer than the cathode (k). Unlike normal incandescent lamps and bulbs which generate large amounts of heat when illuminated, the light emitting diode produces a "cold" generation of light which leads to high efficiencies than the normal "light bulb" because most of the generated energy radiates away within the visible spectrum. Because LEDs are solid-state devices, they can be extremely small and durable and provide much longer lamp life than normal
light sources.

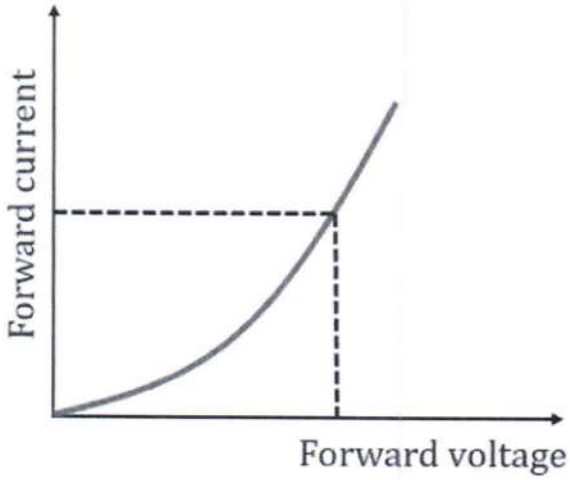

Figure 2.4: V-I Characteristics of LED

2.2.1 Characteristics of LED:

LEDs are solid-state devices. The advantages are:

1) Light Generated by LED is Directional

- LED is all forward directional lighting, not Omni as conventional light bulb.
- In general, beam angel is around 140 degree.
- Utilize this directional characteristics and employee optical lens can achieve

different light patterns.

2) LED can Generate Different Light Color

- Wavelength determinate light color output: red, green, blue, yellow, or purple.
- RGB light mix or different phosphor mix will create white light.

3) Temperature will Affect LED Efficacy

- LED itself will generate heat, which will affect efficacy as well as LED life.
- In general, 10 Degree increase will reduce 5 – 7% lumen output
- Maintain P-N Junction temperature under 75 degree will enable LED last for over 50,000 hours.

4) Low Energy Consumption

- 100 lm/W is commercialized, while over 200lm/W is achieved in lab.
- I Less than 1/5 to 1/10 power consumption of conventional lighting is achieving or 80% to 90% of energy will be saved.

5) Long Life

- No fragile parts, as conventional light bulb, to be broken.
- Light will decay lumen output, but rarely burn out or dead.
- A well-designed luminaire expects over 70% lumen maintenance at 50,000 hours usage.

2.3 LCD (Liquid Crystal Display):

A liquid crystal display or LCD draws its definition from its name itself. It is a combination of two states of matter, the solid and the liquid. LCD uses a liquid crystal to produce a visible image. Liquid crystal displays are super-thin technology. We always use

devices made up of Liquid Crystal Displays (LCDs) like computers, digital watches and also DVD and CD players. They have become very common and have taken a giant leap in the screen industry by clearly replacing the use of Cathode Ray Tubes (CRT). CRT draws more power than LCD and are also bigger and heavier. All of us have seen an LCD, but only few knows how exactly they work.

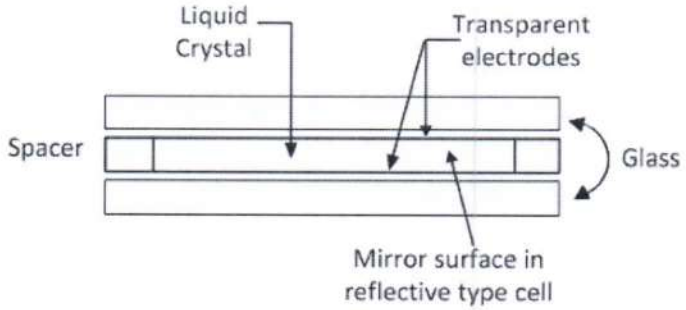

Figure 2.5: LCD Construction

2.3.1 Working Principle of LCD

The working principle of the LCD is of two types. They are the dynamic scattering type and the field effects type. Their details explanation is shown below.

2.3.2 Dynamic Scattering

When the potential carrier flows through the light, the molecular alignment of the liquid crystal disrupts, and they produce disturbances. The liquid becomes transparent when they are not active. But when they are active their molecules turbulence causes scattered of light in all directions, and their cell appears bright. This type of scattering is known as the dynamic scattering. The construction of the dynamic scattering of the liquid crystal cell is shown in the figure.

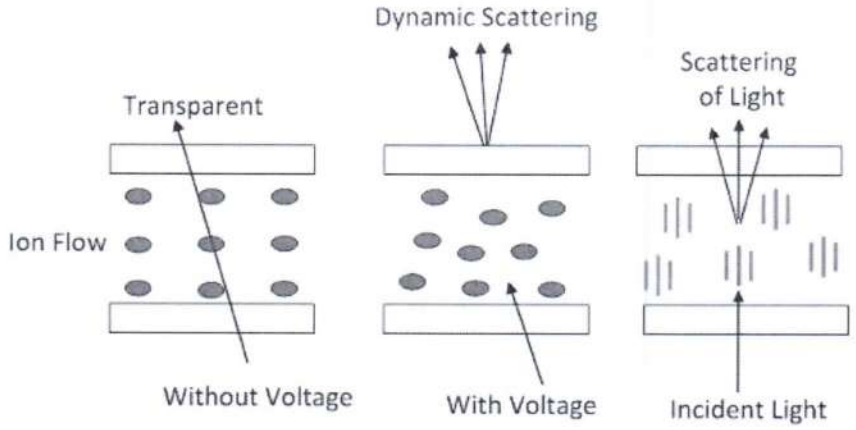

Figure 2.6: Phenomenon of Dynamic scattering

2.3.4 Field Effect Type

The construction of liquid crystals is similar to that of the dynamic scattering types the only difference is that in field effect type LCD the two thin polarising optical fibres are placed inside each glass sheet. The liquid crystals used in field effect LCDs are of different scattering types that operated in the dynamic scattering cell.

The field affects type LCD uses the nematic material which twisted the unenergised light passing through the cell. The nematic type material means the liquid crystals in which the molecules are arranged in parallel but not in a well-defined plane. The light after passing through the nematic material passing through the optical filters and appears bright. When the cell has energised no twisting of light occurs, and the cell appears dull.

The main principle behind liquid crystal molecules is that when an electric current is applied to them, they tend to untwist. This causes a change in the light angle passing through them. This causes a change in the angle of the top polarizing filter with respect to it. So little light is allowed to pass through that particular area of LCD. Thus, that area becomes darker comparing to others. For making an LCD screen, a reflective mirror has to be setup in the back. An electrode plane made of indium-tin oxide is kept on top and a glass with a polarizing film is also added on the bottom side. The entire area of the LCD has to be covered by a common electrode and above it should be the liquid crystal substance. Next comes another piece of glass

with an electrode in the shape of the rectangle on the bottom and, on top, another polarizing film. It must be noted that both of them are kept at right angles. When there is no current, the light passes through the front of the LCD it will be reflected by the mirror and bounced back. As the electrode is connected to a temporary battery the current from it will cause the liquid crystals between the common-plane electrode and the electrode shaped like a rectangle to untwist. Thus, the light is blocked from passing through. Thus, that particular rectangular area appears blank.

2.3.5 Characteristics of LCD:

1. **The resolution of LCD can be very high, and the PPI (pixels per inch) of general mobile phones can reach more than 300.**

2. **LCD grayscale more, can display a wider range of colors.**

3. **TFT LCD high display quality:**

   because the LCD screen every point after receiving the signal has been maintained the color and brightness, constant luminescence, and not like the cathode ray tube display (CRT) need to constantly refresh bright spots. Therefore, the LCD picture quality is high and absolutely does not blink, reducing eye fatigue to a minimum.

4. **TFT LCD screen no electromagnetic radiation:**

   Traditional screen display material is a phosphor, by electron beam phosphors impact, according to the electron beam in the hit for a moment on the fluorescent powder can produce strong electromagnetic radiation, although there are many display products is more effective in the treatment of the radiation on the processing, as much as possible to minimize radiation, but it is difficult to eliminate. Liquid crystal displays (LCDs), by contrast, have an innate advantage in preventing radiation because they do not exist. In the prevention of electromagnetic wave, the LCD screen also has its own unique advantages, it has adopted strict sealing technology will come from the power circuit of the closed a small number of electromagnetic waves in the screen, and the need for ordinary display in order to

CHAPTER-3

BIPOLAR JUNCTION TRANSISTER (BJT)

Content:

Bipolar junction transistor-Types, Symbols and operation, Transistor Current Components, Transistor Equation- Relation among I_C, I_B, I_{CBO}, Transistor configurations- CB, CE and CC, Transistor as switch, Transistor switching times, Transistor as an Amplifier, Characteristics of Transistor in Common Base Configuration, Common Emitter and Common Collector Configurations- Input and output characteristics, Early effect, Transistor parameters, current amplification factor, Relation among α, β and γ, Comparison of CB, CE and CC configurations, Typical transistor junction voltage values.

3. OBJECTIVES

After the completion of this chapter we should be able to understand:

- Able to describe and analyze the transistor characteristics.
- To study the characteristics of transistor in various configurations.
- Current components of transistor to be analyzed.

3.1 BIPOLAR JUNCTION TRANSISTOR-TYPES

Bipolar junction transistors, commonly known as BJT, is a Si or Ge semiconductor device which is structured like two p-n junction diodes connected back to back. It has two outer regions which are the emitter and collector and another region in the middle known as the base. The bipolar junction transistor is called bipolar as both holes and electrons play a fundamental role in its operation.

BJT is a current controlled device, meaning that the current flow through the collector and emitter is controlled by the magnitude of current flowing into the base.

Based on their construction, there are two types of BJTs which are the P-N-P and N-P-N types. These two types of structures operate in a similar way. The only difference is their biasing and the polarity of the power supply for each of the structures. The N-type has extra electrons added to it which causes it to become negative. The P-type has electrons removed from it which result in the formation of holes, therefore giving it a positive charge.

3.2 SYMBOLS AND OPERATION

Emitter: A heavily dope region that passes charged particles to the base.
Base: A thin and lightly dope region. Base passes the charged particles from the emitter to the collector.

Collector: The largest region of a transistor. It is lightly doped than the emitter but heavily doped than the base. Bipolar junction transistors aid in regulating the current flow in a circuit. The current that flows

through the transistor is in proportion to the amount of biasing voltage that is being applied at the base terminal.

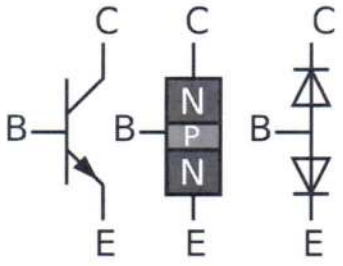

Figure 3.1: Typical BJT

3.2.1 NPN Transistor

The **N-P-N** transistors consist of two N- doped semiconductor layers which act as the emitter and collector and a single P-doped layer which acts as the base. A high current is produced in the collector and emitter when the current at the base is amplified.

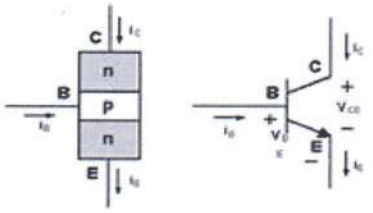

Figure 3.2: NPN Transistor

IE, IB and IC are the emitter and collector current and VEB and VCB are the emitter-base and collector base voltages. According to the sign convention, it can be observed that when the current flows into all the terminals the sign of the current is positive. When the current flows out of the emitter terminal and exits the transistor the sign of the current is negative.

A bipolar junction transistor is that it works as an electron valve. When there is no current flowing in the transistor this is because the p-type silicon semiconductor does not have enough electrons which act as a barrier for the conduction of current to take place. The N-P-N bipolar junction transistor will only work when the electrons flow from a region of low electron junction to an area of high electron junction.

An NPN transistor is considered to be in its ON state when the minority carriers in the P-type region allow the electrons to flow between the collector and emitter terminals of the transistor. This allows a large amount of current to flow in the circuit, therefore resulting in faster operation.

The structure of NPN bipolar junction transistor is shown in the figure. It consists of highly doped N type emitter which is surrounded by a P-type lightly doped base. The collector covers the larger portion of the BJT and surrounds the base and the emitter.

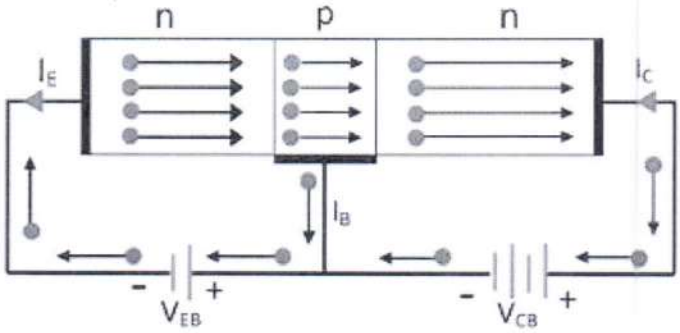

Figure 3.3: Construction of NPN transistor

3.2.2 PNP transistor

The **P-N-P** transistor consists of one N-doped semiconductor layer which is the base and two layers of P-doped semiconductor material which act as the collector and emitter. The amplified base current enters the collector at the output. In the P-N-P the current flow is controlled by the base but the current flow is from emitter to collector.

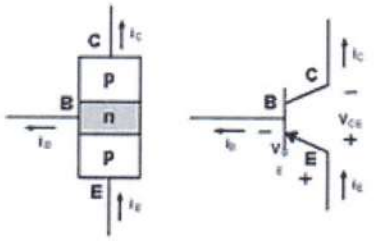

Figure 3.4: PNP Transistor

The P-N-P transistor produces a lower current output compared to the N-P-N transistor because instead of electrons, the emitter emits "holes" which denotes the absence of electrons that are collected by the collector. Hence, the transistor operates much slower and is not used as often as the N-P-N transistor.

The structure of PNP bipolar junction transistor is shown in the figure. It consists of highly doped P type emitter which is surrounded by a N-type lightly doped base. The collector covers the larger portion of the BJT and surrounds the base and the emitter.

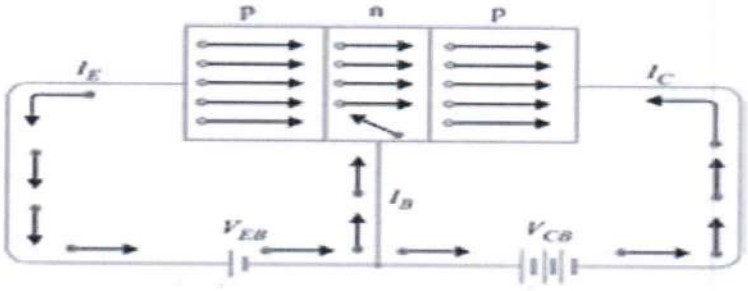

Figure 3.3: Construction of PNP transistor

3. 3 TRANSISTOR CURRENT COMPONENTS

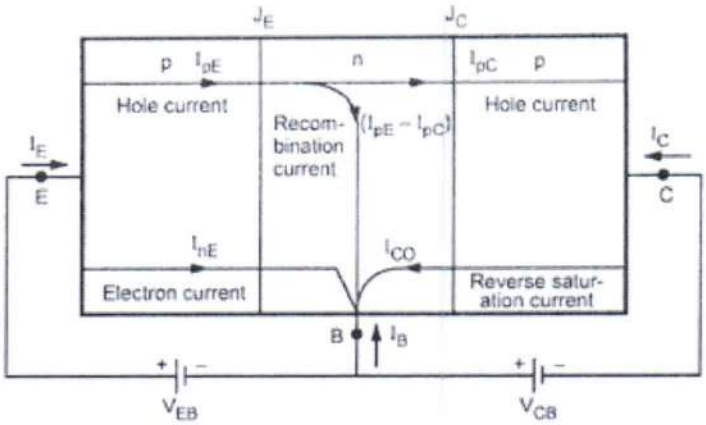

Figure 3.3: Transistor Current Components.

The conduction of current in NPN transistor is owing to electrons and in PNP transistor, it is owing to holes. The direction of current flow will be in opposite direction. Here, we can discuss the current components in a PNP transistor with common base configuration. The emitter-base junction (J_E) is forward biased and the collector-base junction (J_C) is reversed biased as shown in figure. All the current components related to this transistor are shown here. We know that, the current arrives the transistor through the emitter and this current is called emitter current (I_E). This current consists of two constituents – Hole current (I_{hE}) and Electron current (I_{eE}). I_{eE} is due to passage of electrons from base to emitter and IhE is due to passage of holes from emitter to base.

$$I_E = I_{hE} + I_{eE}$$

Some of the holes which are crossing the junction J_E (emitter junction) combines with the electrons present in the base (N-type). Thus, every holes crossing J_E will not arrive at J_C. The remaining holes will reach the collector junction which produces the hole current component, I_{hC}. There will be bulk recombination in the base and the current leaving the base will be

$$I_B = I_{hE} - I_{hC}$$

The electrons in the base which are lost by the recombination with holes (injected into the base across J_E) are refilled by the electrons that enter into the base region. The holes which are arriving at the collector junction (J_C) will cross the junction and it will go into the collector region. When the emitter circuit is open circuited, then $I_E = 0$ and $I_{hC} = 0$. In this condition, the base and collector will perform as reverse biased diode. Here, the collector current, I_C will be same as reverse saturation current (I_{CO} or I_{CBO}). I_{CO} is in fact a small reverse current which passes through the PN junction diode. This is due to thermally generated minority carriers which are pushed by barrier potential. This reverse current increase; if the junction is reverse biased and it will have the same direction as the collector current. This current attains a saturation value (I_0) at moderate reverse biased voltage.

When the emitter junction is at forward biased (in active operation region), then the collector current will become

$$I_C = \alpha I_E + I_{CO}$$

The α is the large signal current gain which is a fraction of the emitter current which comprises of I_{hC}.

When the emitter is at closed condition, then $I_E \neq 0$ and collector current will be

$$I_C = I_{CO} + I_{hC}$$

In a PNP transistor, the reverse saturation current (I_{CBO}) will comprises of the current due to the holes passing through the collector junction from the base to collector region (I_{hCO}) and the current due to the electrons which are passing through the collector junction in the opposite direction (I_{eCO}).

$$Therefore,\ I_{CO} = I_{hCO} + I_{eCO}$$

The total current entering into the transistor will be equal to the total current leaving the transistor (according to Kirchhoff's current law).

$$So,\ I_E = I_C + I_B\ or\ I_E = -(I_C + I_B)$$

.3.1 Parameters Related to Current Components

Relation among I_C, I_B and I_{CBO}:

$I_C = -\alpha I_E + I_{CBO}$

Since I_C and I_E are flowing in opposite directions,

$I_E = -(I_C + I_B)$

Therefore, $I_C = -\alpha [-(I_C + I_B)] + I_{CBO}$

$I_C - \alpha I_C = \alpha I_B + I_{CBO}$

$I_C (1-\alpha) = \alpha I_B + I_{CBO}$

$I_C = \alpha/1-\alpha\ I_B + I_{CBO}/1-\alpha$ (a)

Since $\beta = \alpha/1-\alpha$ (1)

The above expression becomes

$I_C = (1+\beta)\ I_{CBO} + \beta\ I_B$ (2)

Relation among I_C, I_B and I_{CEO}: In the common emitter transistor circuit, I_B is the input current and I_C is the output current. If the base circuit is open, i.e $I_B = 0$, then a small electric current flows from the collector to emitter. This is denoted as I_{CEO}, the collector- emitter current with base open. This current I_{CEO} is also called the collector to emitter leakage current.

In this CE configuration of the transistor, the emitter-base junction is forward-biased and collector-base junction is reverse-biased and hence the collector current I_C is the sum of the part of the emitter current I_E that reaches the collector, and the collector-emitter leakage current I_{CEO}. Therefore the part of I_E, which reaches collector, is equal to (I_C-I_{CEO}).

Hence, the large-signal current gain (β) is defined as,

$\beta = I_C - I_{CEO}/ I_B$ (3)

From the equation, we have

$I_C = \beta I_B = + I_{CEO}$ (4)

Relation between I_{CBO} and I_{CEO}: Comparing equations 2 and 4, we get the relationship between the leakage currents of transistor common-base (CB) and common- emitter (CE) configurations as

$I_{CEO} = (1+\beta)\ C$

From this equation, it is evident that the collector-emitter leakage current (I_{CEO}) in CE configuration is $(1+\beta)$ times larger than that in CB configuration. As I_{CBO} is temperature- dependent, I_{CEO} varies by large amount when temperature of the junction changes.

Expression for Emitter Current:

The magnitude of emitter -current is

$I_E = I_C + I_B$

Substituting equation 2 in the above equation, we get

$I_E = (1+\beta)\, I_{CBO} + (1+\beta)\, I_B$

Substituting equation a in the above equation, we have

$I_E = 1/1-\alpha \;\; I_{CBO} + \;\; 1/1-\alpha \; I_B$

DC Current gain (β_{dc} or h_{FE}): The d.c current gain is defined as the ratio of the collector current I_C to the base current I_B. That is

$\beta_{dc} = h_{FE} = I_C / I_B$

Small Signal Current Gain (α_{ac}):

$$\frac{\Delta I_C}{\Delta I_E}$$

With collector base voltage constant (V_{CB}), it is always positive and it will be less than unity.

3.4 TRANSISTOR CONFIGURATIONS

3.4.1 Working principle of BJT

Since the bipolar junction transistors are made by connecting two diodes back to back, there exist quasi-neutral regions in the emitter, base and collector. These regions remain neutral only at a thermal equilibrium state. This is because when a voltage is supplied the charge densities and electric field in these regions do not change significantly compared to the depletion region. Therefore, for calculating the operation of the BJT these regions are considered neutral. In BJT the emitter to the base junction is forward biased and the collector to the base junction is reverse biased.

When the required voltage is applied to the base, a certain amount of current flows into the base ($\mathbf{I_B}$). This turns on the transistor and which in turn allows current flow from the collector to the emitter (Assuming that the transistor is NPN type). Let us assume that the base-emitter junction is forward biased and the base-collector junction is reverse biased. The following phenomenon occurs inside the transistor:

- Since the base-emitter junction is forward biased, the positively charged holes from the lightly doped base move through the PN junction to the emitter.
- Also, the forward bias reduces the barrier potential of the base-emitter junction. Hence, a small amount of electrons (nearly 1%) from the emitter crosses the base-emitter junction to reach the

lightly doped base and recombines with the holes in the base.

- The remaining electrons in the emitter (about 99%) cross the base-emitter junction and pass through the base-collector junction resulting in electron flow from the emitter to the collector. This constitutes the collector current I_B.

  $I_E=I_C+ I_B$

- A similar phenomenon occurs in PNP transistor, but the electrons are replaced by holes and holes are replaced by electrons.

3.4.2 Operation regions of BJT

BJT can act as either insulators or conductors depending on the base current. This gives them the ability to change between two varying states that are switching and amplification. Therefore, the BJT can operate in three operational modes which are:

Active region: – When the transistor operates in the active region it acts as an amplifier where $I_C = \beta.I_B$

Saturation region: – In this region, the transistor is in a full "ON state" and operates as a switch. Here the collector current is equivalent to the saturation current.

Cut-Off region: – In the cut-off region the transistor in a full "OFF state" and operates as a switch. No collector current flows through the circuit.

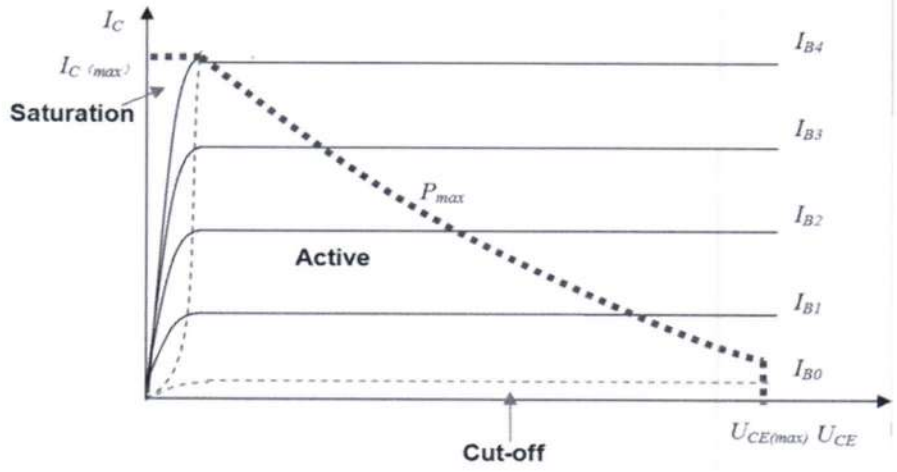

Figure 3.4: VI- Characteristics of BJT

The controlled current flows between the emitter and collector and the controlling current flow to the base. Therefore, a small base current controls the larger collector current. When the base has no current flowing through it then it is in a cut off state. When the transistor has maximum current flowing through it then it is said to be in the saturation region and is in a fully conducting state.

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3.4.3 Bipolar Transistor Configurations

As the Bipolar Transistor is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor varies with each circuit arrangement.

- **Common Base Configuration** – has Voltage Gain but no Current Gain.
- **Common Emitter Configuration** – has both Current and Voltage Gain.
- **Common Collector Configuration** – has Current Gain but no Voltage Gain.

3.4.4 The Common Base (CB) Configuration

As its name suggests, in the Common Base or grounded base configuration, the BASE connection is common to both the input signal AND the output signal. The input signal is applied between the transistors base and the emitter terminals, while the corresponding output signal is taken from between the base and the collector terminals as shown. The base terminal is grounded or can be connected to some fixed reference voltage point.

The input current flowing into the emitter is quite large as its the sum of both the base current and collector current respectively therefore, the collector current output is less than the emitter current input resulting in a current gain for this type of circuit of "1" (unity) or less, in other words the common base configuration "attenuates" the input signal.

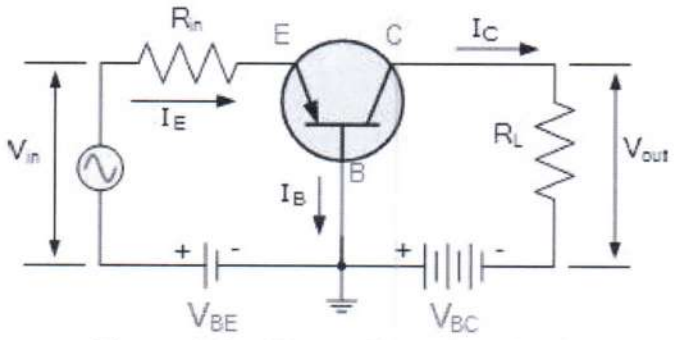


Figure 3.5: CB- configuration circuit

This type of amplifier configuration is a non-inverting voltage amplifier circuit, in that the signal voltages V_{in} and V_{out} are "in-phase". This type of transistor arrangement is not very common due to its unusually high voltage gain characteristics. Its input characteristics represent that of a forward biased diode while the output characteristics represent that of an illuminated photo-diode.

Also this type of bipolar transistor configuration has a high ratio of output to input resistance or more importantly "load" resistance (R_L) to "input" resistance (R_{in}) giving it a value of "Resistance Gain". Then the voltage gain (Av) for a common base configuration is therefore given as ratio of output voltage to input voltage.

3.4.5 The Common Emitter (CE) Configuration

In the Common Emitter or grounded emitter configuration, the input signal is applied between the base and the emitter, while the output is taken from between the collector and the emitter as shown. This type of configuration is the most commonly used circuit for transistor based amplifiers and which represents the "normal" method of bipolar transistor connection.

The common emitter amplifier configuration produces the highest current and power gain of all the three bipolar transistor configurations. This is mainly because the input impedance is LOW as it is connected to a forward biased PN-junction, while the output impedance is HIGH as it is taken from a reverse biased PN-junction.

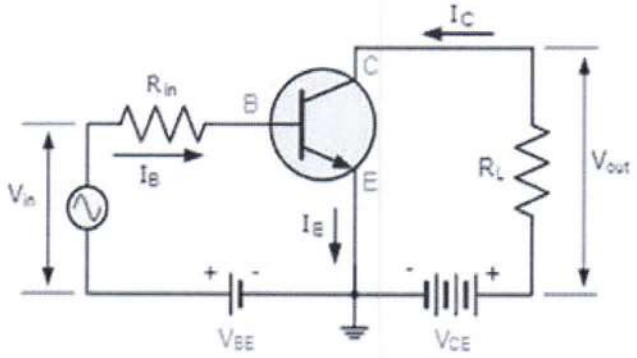


Figure 3.6: CE configuration circuit

In this type of configuration, the current flowing out of the transistor must be equal to the currents flowing into the transistor as the emitter current is given as Ie = Ic + Ib. As the load resistance (RL) is connected in series with the collector, the current gain of the common emitter transistor configuration is quite large as it is the ratio of Ic/Ib. A transistors current gain is given the Greek symbol of Beta, (β).

As the emitter current for a common emitter configuration is defined as Ie = Ic + Ib, the ratio of Ic/Ie is called Alpha, given the Greek symbol of α. Note: that the value of Alpha will always be less than unity. Since the electrical relationship between these three currents, Ib, Ic and Ie is determined by the physical construction of the transistor itself, any small change in the base current (Ib), will result in a much larger change in the collector current (Ic).

Then, small changes in current flowing in the base will thus control the current in the emitter-collector circuit. Typically, Beta has a value between 20 and 200 for most general purpose transistors. So if a transistor has a Beta value of say 100, then one electron will flow from the base terminal for every 100 electrons flowing between the emitter-collector terminals.

3.4.6 The Common Collector (CC) Configuration

In the Common Collector or grounded collector configuration, the collector is connected to ground through the supply, thus the collector terminal is common to both the input and the output. The input signal

is connected directly to the base terminal, while the output signal is taken from across the emitter load resistor as shown. This type of configuration is commonly known as a Voltage Follower or Emitter Follower circuit.

The common collector or emitter follower configuration is very useful for impedance matching applications because of its very high input impedance, in the region of hundreds of thousands of Ohms while having a relatively low output impedance.

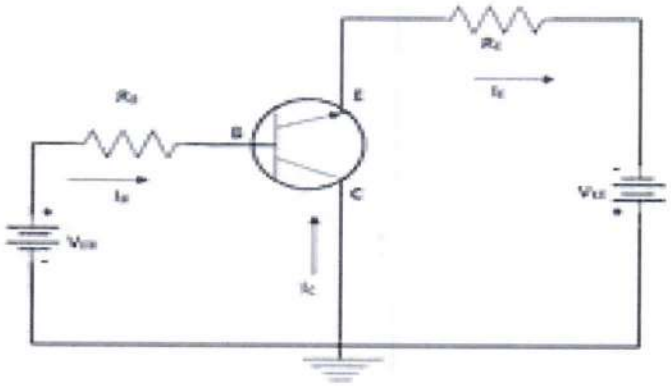


Figure 3.7: CC configuration circuit

The common emitter configuration has a current gain approximately equal to the β value of the transistor itself. However in the common collector configuration, the load resistance is connected in series with the emitter terminal so its current is equal to that of the emitter current. As the emitter current is the combination of the collector AND the base current combined, the load resistance in this type of transistor configuration also has both the collector current and the input current of the base flowing through it.

3.5 BIPOLAR JUNCTION TRANSISTOR (BJT) SWITCH

The Bipolar Junction Transistor can be used as a switch. This is required when the typical digital output (max current output 20ma) does not provide sufficient current drive for high current devices like lamps, solenoids or motors. The transistor current gain provides the order of magnitude increase in collector current.

There are two main regions in the operation of a transistor which we can consider as **ON** and **OFF** states. They are saturation and cut **off** states. Let us have a look at the behavior of a transistor in those two states.

3.5.1 Operation in Cut-off condition

The following figure shows a transistor in cut-off region.

UNIT IV

BJT BIASING AND THERMAL STABILITY

CONTENT:

Need for Biasing, Operating point, Load Line Analysis – D.C. Load Line, A.C Load Line, and Biasing - Methods, Basic Stability, Fixed Bias, Collector-to-base and self-Bias.

4.0 OBJECTIVES

After the completion of this chapter we should be able to understand:

- To know the need of biasing for transistors and Q point analysis.
- To know the A.C. and D.C. analysis of amplifiers.
- To know the factors those influence the stability of transistors.
- Various biasing techniques of the transistors to studies.

4.1 BIASING AND NEED FOR BIASING

Biasing is the process of providing DC voltage which helps in the functioning of the circuit. A transistor is based in order to make the emitter base junction forward biased and collector base junction reverse biased, so that it maintains in active region, to work as an amplifier. In the previous chapter, we explained how a transistor acts as a good amplifier, if both the input and output sections are biased.

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Due to this reason for a BJT, to amplify a signal two conditions have to be met.

- The input voltage should exceed cut-in voltage for the transistor to be ON.
- The BJT should be in the active region, to be operated as an amplifier.

If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this problem can be avoided. The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed.

The below figure shows a transistor amplifier, that is provided with DC biasing on both input and output circuits.

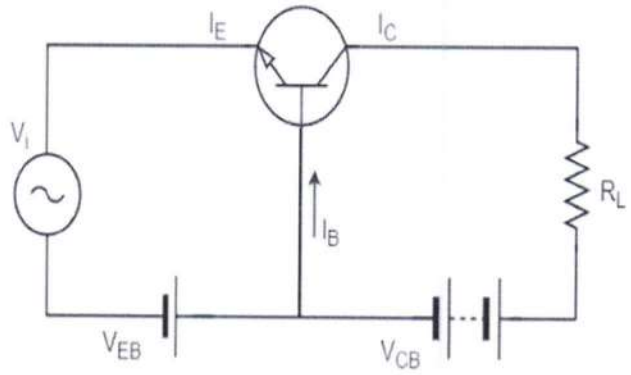


Figure 4.1: Typical BJT biasing circuit

For a transistor to be operated as a faithful amplifier, the operating point should be stabilized. Let us have a look at the factors that affect the stabilization of operating point.

4.2 OPERATING POINT

The point which is obtained from the values of the IC (collector current) or VCE (collector-emitter voltage) when no signal is given to the input is known as the operating point or Q-point in a transistor. It is called operating point because variations of IC (collector current) and VCE (collector-emitter voltage) takes place around this point when no signal is applied to the input. The operating point is also called quiescent (silent) point or simply Q-point because it is a point on IC – VCE characteristic when the transistor is silent, or no input signal is applied to the circuit. The operating point can be easily obtained by the DC load line method. The DC load line

is explained below.

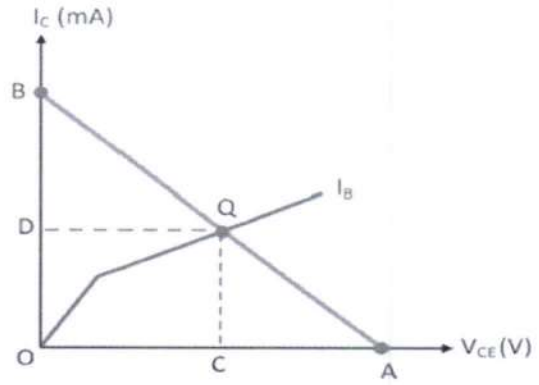


Figure 4.2: Operating point of Transistor

Let, determines the operating point of particular base circuit current I_B. According to the load line condition, the OA = V_{CE} = V_{CC} and OB = I_C = V_{CC}/R_C is shown on the output characteristic curve above. The point Q is the operating point where the DC load line intersects the base current I_B at the output characteristic curves in the absence of input signal.

Where I_C= OD mA

V_{CE} = OC volts.

The position of the Q-point depends on the applications of the transistor. If the transistor is used as a switch, then for open switch the Q-point is in the cutoff region, and for the close switch, the Q-point is in the saturation region. The Q-point lies in the middle of the line for the transistor which operates as an amplifier.

Note: In saturation region, both the collector base region and the emitter-base region are in forward biased and heavy current flow through the junction. And the region in which both the junctions of the transistor are in reversed biased is called the cut-off region.

4.3 LOAD LINE ANALYSIS

The load line analysis of transistor means for the given value of collector-emitter voltage we find the value of collector current. This can be done by plotting the output characteristic and

then determine the collector current IC with respect to collector-emitter voltage VCE. The load line analysis can easily be obtained by determining the output characteristics of the load line analysis methods.

4.3.1 D.C. Load Line Analysis:

The DC load represents the desirable combinations of the collector current and the collector-emitter voltage. It is drawn when no signal is given to the input, and the transistor becomes bias.

Consider a CE NPN transistor circuit shown in the figure below where no signal is applied to the input side. For this circuit, DC condition will obtain, and the output characteristic of such a circuit is shown in the figure below.

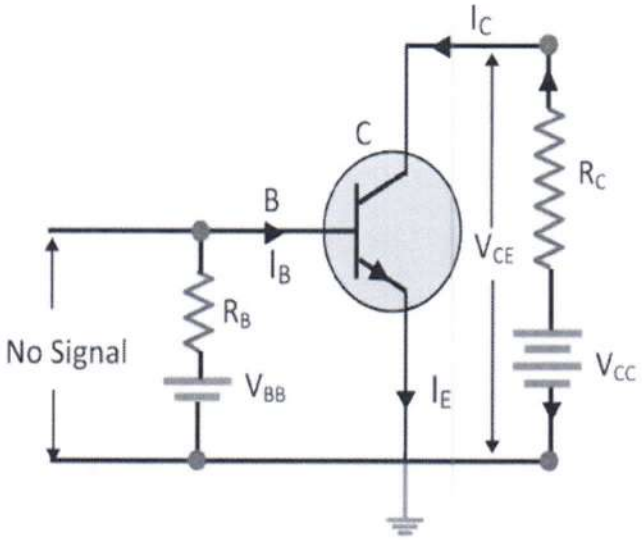


Figure 4.3: Circuit for DC Load line

The DC load line curve of the above circuit is shown in the figure below.

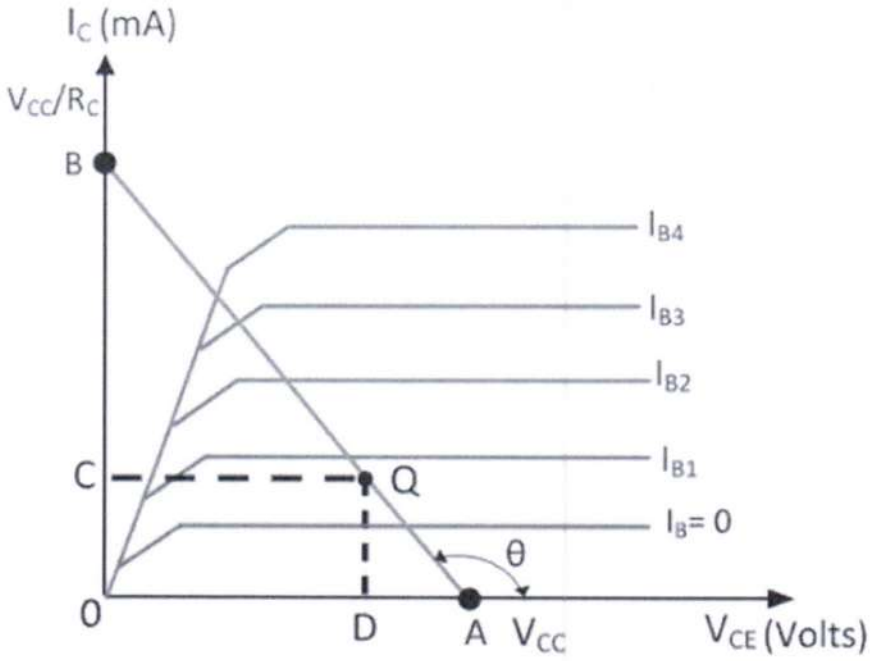


Figure 4.4: DC Load line

By applying Kirchhoff's voltage law to the collector circuit, we get,

$$V_{CC} = V_{CE} + I_C R_C \quad \text{.....(1)}$$

$$V_{CE} = V_{CC} - I_C R_C \quad \text{.....(2)}$$

The above equation shows that the V_{CC} and R_C are the constant value, and it is the first-degree equation which is represented by the straight line on the output characteristic. This load line is known as a DC load line. The input characteristic is used to determine the locus of V_{CE} and I_C point for the given value of R_C. The end point of the line are located as

1. The collector-emitter voltage V_{CE} is maximum when the collector current $I_C = 0$ then from the equation (1) we get,

$$V_{CE} = V_{CC} - 0 \times R_C \quad \text{..... (3)}$$

$$V_{CE} = V_{CC} \quad \text{..... (4)}$$

The first point A (OA = V_{CC}) on the collector-emitter voltage axis shown in the figure above.

2. The collector current I_C becomes maximum when the collector-emitter voltage $V_{CE} = 0$ then from the equation (1) we get.

$$0 = V_{CC} - I_C R_C \quad \text{..... (5)}$$

$$I_C = \frac{V_{CC}}{R_C} \quad \text{..... (6)}$$

This gives the second point on the collector current axis as shown in the figure above. By adding the points A and B, the DC load line is drawn. With the help of load line, any value of collector current can be determined.

4.3.1 AC Load Line

AC Equivalent Circuits – Capacitors behave as short-circuits to ac signals, so in the ac equivalent circuit for a transistor circuit all capacitors must be replaced with short-circuits. Power supplies also behave as ac short-circuits, because the dc supply voltage is not affected by ac signals. Also, all power supplies have large-value capacitors at the output terminals and these will offer short-circuits to ac signals. Substituting short-circuits in place of the power supply and all capacitors in the circuit in figure gives the ac equivalent circuit in figure. If R_L is present, as shown, it appears in parallel with R_C in the ac equivalent circuit of AC Load Line of BJT.

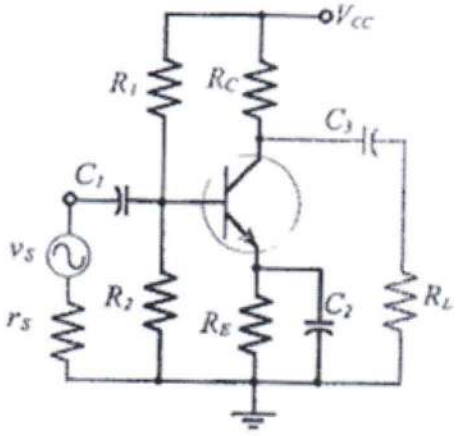


Figure 4.5a: Circuit with coupling and Bypass capacitors

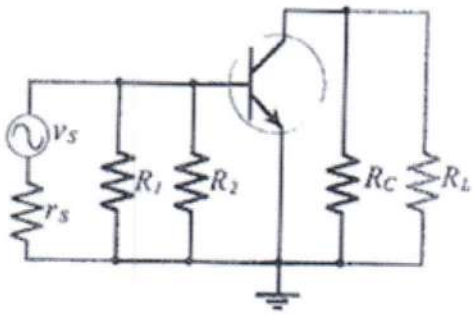


Figure 4.5b: Power supply and capacitors behaves as ac short circuit

Figure 4.5: AC Load line

Once the ac equivalent circuit is drawn, the circuit ac performance can be investigated by drawing an AC Load Line of BJT, and by substituting a transistor model in place of the device.

The dc load for the circuit in Fig. 4.5 (a) is ($R_C + R_E$), consequently, the dc load line is drawn for a total resistance of ($R_C + R_E$). Because the emitter resistor is capacitor bypassed in above figure (a), resistor R_E is not part of the circuit ac load. If external load R_L were not present, the circuit ac load would simply be R_C. With R_L capacitor-coupled to the circuit output, the ac load is $R_C \| R_L$. An AC Load Line of BJT may now be drawn to represent the circuit ac performance.

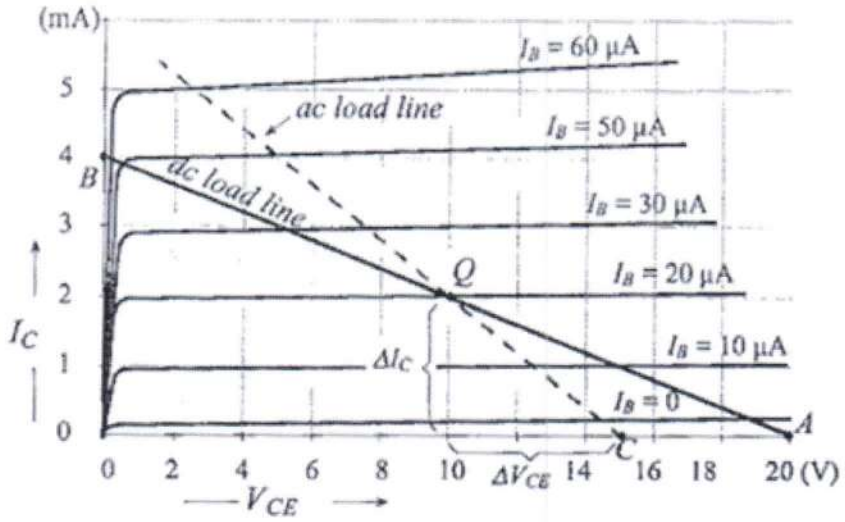


Figure 4.5: The ac load line for a transistor circuit is drawn through the Q-point.

When there is no input signal, the transistor voltage and current conditions are exactly indicated by the Q-point on the dc load line. An a. c signal causes the transistor voltage and current levels to vary above and below the Q-point. Therefore, the Q-point is common to both the ac and dc load lines. Starting from the Q-point, another point is found on the AC Load Line of BJT by taking a convenient collector current change (usually $\Delta I_C = I_{CQ}$) and calculating the corresponding collector-emitter voltage change (ΔV_{CE}) as shown in the above figure.

4.4 TRANSISTOR BIASING METHODS

In this chapter, we will go over the different ways in which a bipolar junction transistor (BJT) can be biased so that it can produce a stable and accurate output signal. Transistor biasing is the controlled amount of voltage and current that must be given to a transistor for it to produce the desired amplification or switching effect. In other words, transistors must be fed the correct or appropriate levels of voltages and/or currents to their various regions in order to function properly and amplify signals to the correct level. This controlled amount of voltage and/or currents fed to the different junctions of a transistor is transistor biasing.

Without appropriate transistor biasing, the transistor may not function at all or amplify very poorly, such as produce clipping of the signal or produce too low of gain. Therefore, it's very important that a transistor is biased correctly for it to produce the intended output effect.

4.4.1 Fixed Bias (Base Bias)

Base bias is the simplest way to bias a BJT transistor. Base bias ensures that the voltage fed to the base, VBB, is the correct voltage, which then supplies the correct current so that the BJT has enough base current to switch the transistor ON, below is a typical BJT receiving base bias:

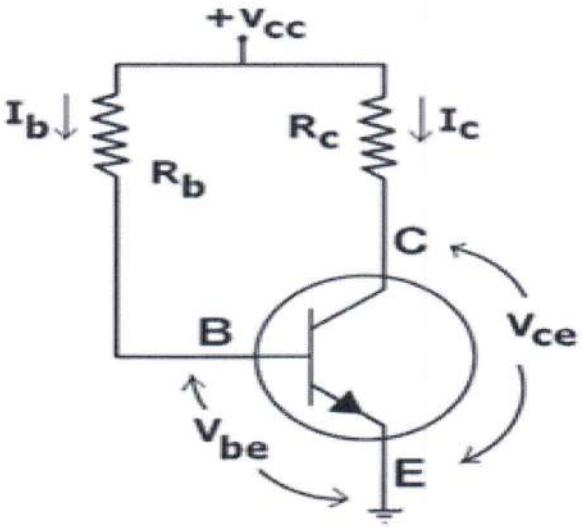


Figure 4.6: Circuit diagram for Fixed Bias (Base Bias)

V_{BB} is the base supply voltage, which is used to give the transistor sufficient current to turn the transistor on. R_B is a resistance value that is used to provide the desired value of base current I_B. V_{CC} is the collector supply voltage, which is required for a transistor to have sufficient power to operate. This voltage is reverse-biases the transistor. Hence the transistor has sufficient power to have an amplified output collector current. The collector resistor, RC provides the desired voltage in the collector circuit. Using the base biasing method, the collector current IC is dependent only on the values of βdc and IB. βdc is the amplification factor by which the base current gets amplified by. So the total output current, I_C will be $I_C=\beta dc \times I_B$.

i. Base Bias Voltage/Current Calculations

When using any biasing technique, calculations must be made of the various voltages and currents through a BJT transistor. Or else, it's impossible to tell whether the voltage and current values are correct or not.

The first calculation we will make is for the base current I_B.

The base current can be found by dividing the voltage across resistor RB by the value of RB

$$I_B = (V_{BB} - V_{BE})/R_B \ldots\ldots\ldots (7)$$

Since the voltage drop across a silicon junction is 0.7V, the value of V_{BE}=0.7V. Therefore, I_B equals:

$$I_B = (V_{BB} - V_{BE})/R_B = (5v - 0.7v)/56k\Omega = 76.78\mu A \ldots\ldots (8)$$

I_C is calculated as:

$$I_C = \beta dc \times I_B = 100 \times 76.78\mu A \approx 7.68mA \ldots\ldots (9)$$

With IC then known, the collector-emitter voltage, VCE can be calculated. This is shown below:

$$V_{CE} = V_{CC} - I_C \times R_C = 15v - (7.68mA \times 1K\Omega) = 7.32v \ldots\ldots\ldots\ldots (10)$$

Base bias can also be done with a single supply voltage, VCC, with VBB omitted. So instead of using VBB in calculations, you would just use VCC instead. The result of the calculations is still same

Disadvantages of Base Bias Method

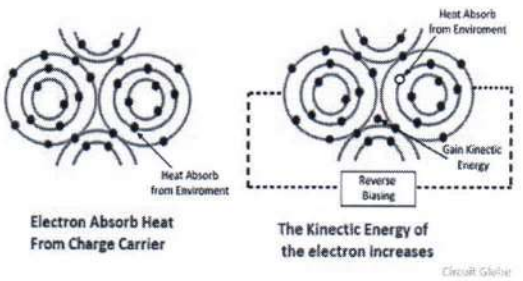
Though base bias is one of the simplest and easiest methods to bias transistors, it is the least popular way to do so. This is because the collector current, IC, is decided by purely by the βdc of the transistor. βdc of a transistor is one of the most unstable and unpredictable parameters of a

Power Point Presentation Slides

BREAK DOWN MECHANISM

Difference Between Avalanche & Zener Breakdown

- **Avalanche breakdown** occurs because of the collision of the electrons, whereas the
- **Zener breakdown** occurs because of the high electric field



Avalanche Breadown

- When the reverse biased applied across the junction, the kinetic energy of the electrons increases and they starts moving at high velocity.
- While moving, they collide with the other atoms and creates the number of free electrons which causes the reverse saturation current.
- Because of this saturation current, the avalanche breakdown mechanism occurs in the diode.

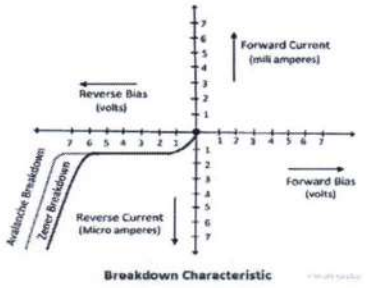
Zener break down

- The Zener breakdown takes place in heavily doped diodes.
- When the high electric field applied across the diode, the electrons start moving across the junction.
- Thus develop the small reversed bias current. When the jumping of electrons increases beyond the rated capacity of the diode, then avalanche breakdown occurs which breaks the junction.
- Thus, as long as the current in the diode is limited the Zener diode will not destroy the junction. But avalanche breakdown destroys the junction.

Avalanche Vs Zener

	Avalanche	Zener Breakdown
Definition	The avalanche breakdown is a phenomena of increasing the free electrons or electric current in semiconductor and insulating material by applying the higher voltage.	The process in which the electrons are moving across the barrier from the valence band of the p-type material to the conduction band of the lightly filled n-material is known as the Zener breakdown.
Depletion Region	Thick	Thin
Junction	Destroy	Not Destroy
Electric Field	Weak	Strong

Produces	Pairs of electron and hole.	Electrons.
Doping	Low	Heavy
Reverse potential	High	Low
Temperature Coefficient	Positive	Negative
Ionization	Because of collision	Because of Electric Field
Breakdown Voltage	Directly proportional to temperature.	Inversely proportional to temperature.
After Breakdown	Voltage vary.	Voltage remains constant



Breakdown Characteristic

LED,LCD

- -Construction
- -Operation
- -Applications

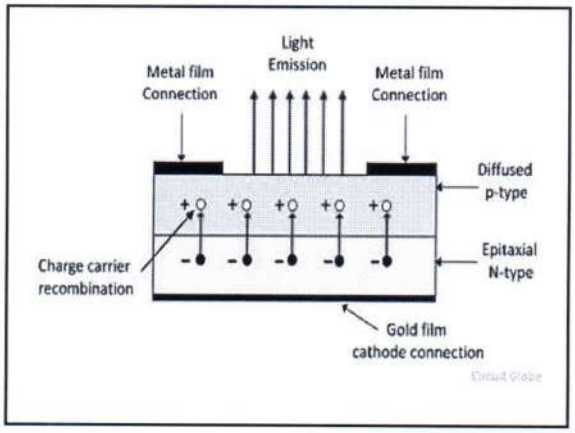
Light Emitting Diode (LED)

- **Definition:** The LED is a PN-junction diode which emits light when an electric current passes through it in the forward direction.
- In the LED, the recombination of charge carrier takes place. The electron from the N-side and the hole from the P-side are combined and gives the energy in the form of heat and light.
- The LED is made of semiconductor material which is colourless, and the light is radiated through the junction of the diode.

- The LEDs are extensively used in segmental and dot matrix displays of numeric and alphanumeric character.
- The several LEDs are used for making the single line segment while for making the decimal point single LED is used.

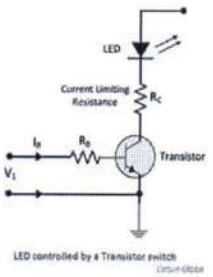
Construction of LED

- The recombination of the charge carrier occurs in the P-type material, and hence P-material is the surface of the LED.
- For the maximum emission of light, the anode is deposited at the edge of the P-type material. The cathode is made of gold film, and it is usually placed at the bottom of the N-region.
- This gold layer of cathode helps in reflecting the light to the surface.



- The gallium arsenide phosphide is used for the manufacturing of LED which emits red or yellow light for emission.
- The LED are also available in green, yellow amber and red in colour.

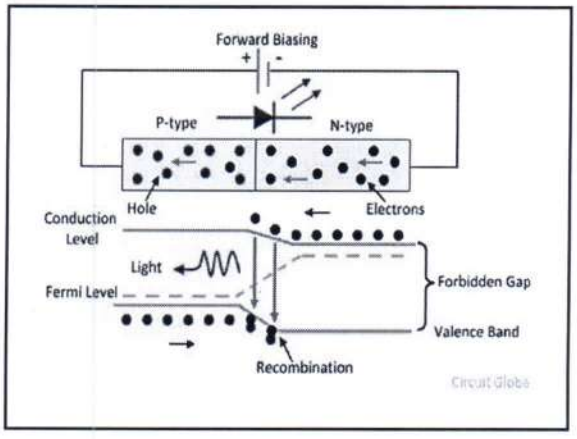
LED controlled by a Ttansistor



- The simple transistor can be used for off/on of a LED as shown in the figure . The base current I_B conducts the transistor, and the transistor conducts heavily. The resistance R_C limits the current of the LED.

Working of LED

- The working of the LED depends on the quantum theory.
- The quantum theory states that when the energy of electrons decreases from the higher level to lower level, it emits energy in the form of photons.
- The energy of the photons is equal to the gap between the higher and lower level.

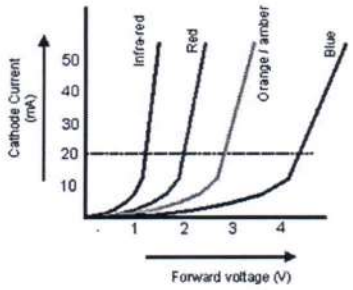


- The LED is connected in the forward biased, which allows the current to flows in the forward direction. The flow of current is because of the movement of electrons in the opposite direction.
- The recombination shows that the electrons move from the conduction band to valence band and they emits electromagnetic energy in the form of photons.
- The energy of photons is equal to the gap between the valence and the conduction band.

Types of Light Emitting Diodes

- Gallium Arsenide (GaAs) – infra-red
- Gallium Arsenide Phosphide (GaAsP) – red to infra-red, orange
- Aluminium Gallium Arsenide Phosphide (AlGaAsP) – high-brightness red, orange-red, orange, and yellow
- Gallium Phosphide (GaP) – red, yellow and green
- Aluminium Gallium Phosphide (AlGaP) – green
- Gallium Nitride (GaN) – green, emerald green
- Gallium Indium Nitride (GaInN) – near-ultraviolet, bluish-green and blue
- Silicon Carbide (SiC) – blue as a substrate
- Zinc Selenide (ZnSe) – blue
- Aluminium Gallium Nitride (AlGaN) – ultraviolet

I-V Characteristics of LED



two types of LED configurations

- The standard configurations of LED are two like emitters as well as COBs
- The emitter is a single die that is mounted toward a circuit board, then to a heat sink. This circuit board gives electrical power toward the emitter, while also drawing away heat.
- To aid in reducing cost as well as enhance light uniformity, investigators determined that the LED substrate can be detached & the single die can be mounted openly to the circuit board. So this design is called COB (chip-on-board array).

Advantages of LED's

- The cost of LED's is less and they are tiny.
- By using the LED's electricity is controlled.
- The intensity of the LED differs with the help of the microcontroller.
- Long Lifetime
- Energy efficient
- No warm-up period

- Rugged
- Doesn't affect by cold temperatures
- Directional
- Color Rendering is Excellent
- Environmentally friendly
- Controllable

Disadvantages of LED's

- Price
- Temperature sensitivity
- Temperature dependence
- Light quality
- Electrical polarity
- Voltage sensitivity
- Efficiency droop
- Impact on insects

Applications of Light Emitting Diode

There are many applications of LED and some of them are explained below.

- LED is used as a bulb in the homes and industries
- The light-emitting diodes are used in motorcycles and cars
- These are used in mobile phones to display the message
- At the traffic light signals led's are used

Chapter 6:
Field-Effect Transistors

FETs vs. BJTs

Similarities:
- Amplifiers
- Switching devices
- Impedance matching circuits

Differences:
- FETs are voltage controlled devices. BJTs are current controlled devices.
- FETs have a higher input impedance. BJTs have higher gains.
- FETs are less sensitive to temperature variations and are more easily integrated on ICs.
- FETs are generally more static sensitive than BJTs.

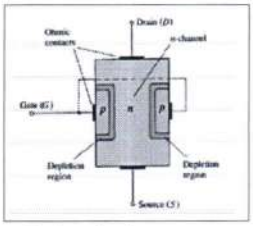
FET Types

- **JFET: Junction FET**
- **MOSFET: Metal–Oxide–Semiconductor FET**
  - **D-MOSFET: Depletion MOSFET**
  - **E-MOSFET: Enhancement MOSFET**

JFET Construction

There are two types of JFETs
- ***n*-channel**
- ***p*-channel**

The n-channel is more widely used.



There are three terminals:
- **Drain (D) and Source (S) are connected to the *n*-channel**
- **Gate (G) is connected to the *p*-type material**

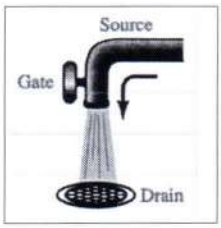
JFET Operation: The Basic Idea

JFET operation can be compared to a water spigot.

The source of water pressure is the accumulation of electrons at the negative pole of the drain-source voltage.

The drain of water is the electron deficiency (or holes) at the positive pole of the applied voltage.

The control of flow of water is the gate voltage that controls the width of the n-channel and, therefore, the flow of charges from source to drain.



JFET Operating Characteristics

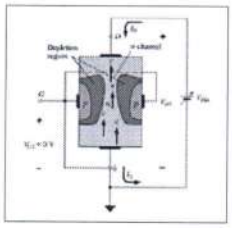
There are three basic operating conditions for a JFET:

- **$V_{GS} = 0$, V_{DS} increasing to some positive value**
- **$V_{GS} < 0$, V_{DS} at some positive value**
- **Voltage-controlled resistor**

JFET Operating Characteristics: $V_{GS} = 0$ V

Three things happen when $V_{GS} = 0$ and V_{DS} is increased from 0 to a more positive voltage

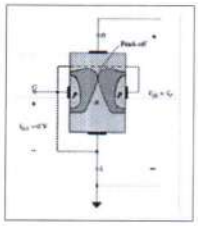
- The depletion region between p-gate and n-channel increases as electrons from n-channel combine with holes from p-gate.
- Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.
- Even though the n-channel resistance is increasing, the current (I_D) from source to drain through the n-channel is increasing. This is because V_{DS} is increasing.



JFET Operating Characteristics: Pinch Off

If $V_{GS} = 0$ and V_{DS} is further increased to a more positive voltage, then the depletion zone gets so large that it pinches off the n-channel.

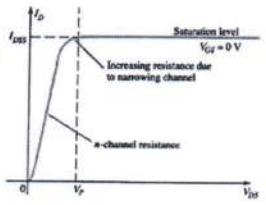
This suggests that the current in the n-channel (I_D) would drop to 0A, but it does just the opposite–as V_{DS} increases, so does I_D.



JFET Operating Characteristics: Saturation

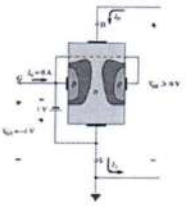
At the pinch-off point:

- Any further increase in V_{GS} does not produce any increase in I_D. V_{GS} at pinch-off is denoted as V_p.
- I_D is at saturation or maximum. It is referred to as I_{DSS}.
- The ohmic value of the channel is maximum.



JFET Operating Characteristics

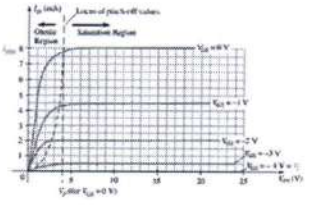
As V_{GS} becomes more negative, the depletion region increases.



JFET Operating Characteristics

As V_{GS} becomes more negative:

- The JFET experiences pinch-off at a lower voltage (V_p).
- I_D decreases ($I_D < I_{DSS}$) even though V_{DS} is increased.
- Eventually I_D reaches 0 A. V_{GS} at this point is called V_p or $V_{GS(off)}$.



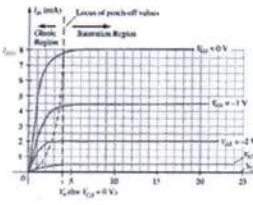
Also note that at high levels of V_{DS} the JFET reaches a breakdown situation. I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

JFET Operating Characteristics: Voltage-Controlled Resistor

The region to the left of the pinch-off point is called the ohmic region.

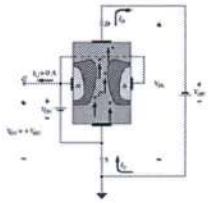
The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d). As V_{GS} becomes more negative, the resistance (r_d) increases.

$$r_d = \frac{r_0}{\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$



p-Channel JFETS

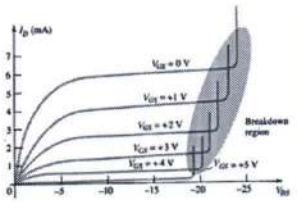
The *p*-channel JFET behaves the same as the *n*-channel JFET, except the voltage polarities and current directions are reversed.



p-Channel JFET Characteristics

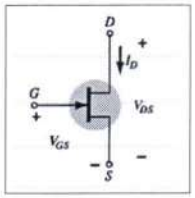
As V_{GS} increases more positively

- The depletion zone increases
- I_D decreases ($I_D < I_{DSS}$)
- Eventually $I_D = 0$ A



Also note that at high levels of V_{DS} the JFET reaches a breakdown situation: I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

N-Channel JFET Symbol



JFET Transfer Characteristics

The transfer characteristic of input-to-output is not as straightforward in a JFET as it is in a BJT.

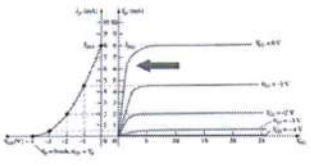
In a BJT, β indicates the relationship between I_B (input) and I_C (output).

In a JFET, the relationship of V_{GS} (input) and I_D (output) is a little more complicated:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

JFET Transfer Curve

This graph shows the value of I_D for a given value of V_{GS}.



Plotting the JFET Transfer Curve

Using I_{DSS} and Vp ($V_{GS(off)}$) values found in a specification sheet, the transfer curve can be plotted according to these three steps:

Step 1

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Solving for $V_{GS} = 0$V $\quad I_D = I_{DSS}$

Step 2

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

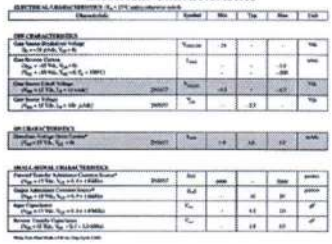
Solving for $V_{GS} = V_p$ ($V_{GS(off)}$) $\quad I_D = 0$A

Step 3

Solving for $V_{GS} = 0$V to V_p $\quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

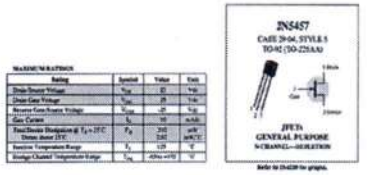
JFET Specifications Sheet

Electrical Characteristics



JFET Specifications Sheet

Maximum Ratings



more...

Case and Terminal Identification

Testing JFETs

- **Curve Tracer**
  A curve tracer displays the I_D versus V_{DS} graph for various levels of V_{GS}.
- **Specialized FET Testers**
  These testers show I_{DSS} for the JFET under test.

MOSFETs

MOSFETs have characteristics similar to JFETs and additional characteristics that make then very useful.

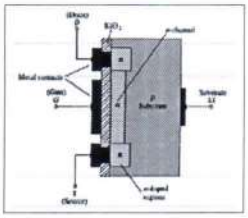
There are two types of MOSFETs:

- **Depletion-Type**
- **Enhancement-Type**

Depletion-Type MOSFET Construction

The Drain (D) and Source (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel. This *n*-channel is connected to the Gate (G) via a thin insulating layer of SiO_2.

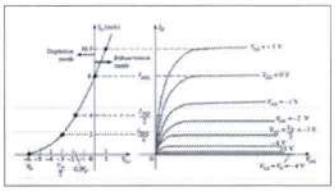
The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called Substrate (SS).



Basic MOSFET Operation

A depletion-type MOSFET can operate in two modes:

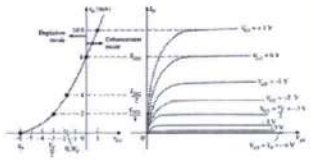
- Depletion mode
- Enhancement mode



D-Type MOSFET in Depletion Mode

Depletion Mode

The characteristics are similar to a JFET.



- When $V_{GS} = 0$ V, $I_D = I_{DSS}$
- When $V_{GS} < 0$ V, $I_D < I_{DSS}$
- The formula used to plot the transfer curve still applies:

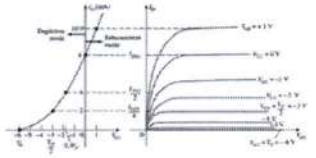
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

D-Type MOSFET in Enhancement Mode

Enhancement Mode

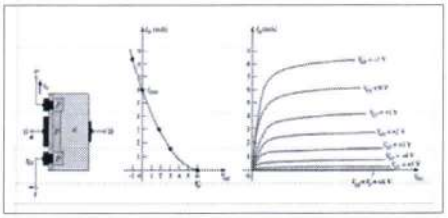
- $V_{GS} > 0$ V
- I_D increases above I_{DSS}
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

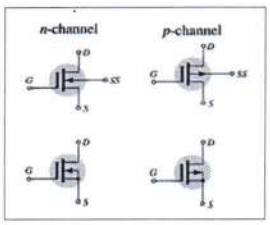


Note that V_{GS} is now a positive polarity

p-Channel D-Type MOSFET



D-Type MOSFET Symbols



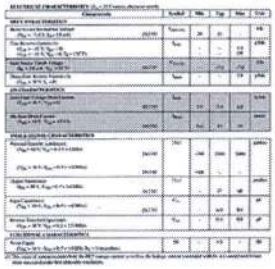
Specification Sheet

Maximum Ratings

more...

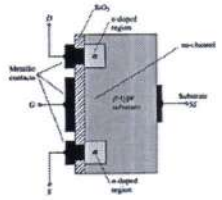
Specification Sheet

Electrical Characteristics



E-Type MOSFET Construction

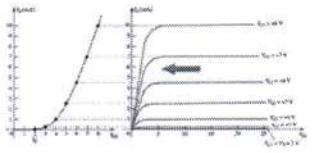
- The Drain (D) and Source (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel
- The Gate (G) connects to the *p*-doped substrate via a thin insulating layer of SiO_2
- There is no channel
- The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called the Substrate (SS)



Basic Operation of the E-Type MOSFET

The enhancement-type MOSFET operates only in the enhancement mode.

- V_{GS} is always positive
- As V_{GS} increases, I_D increases
- As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level, V_{DSsat} is reached

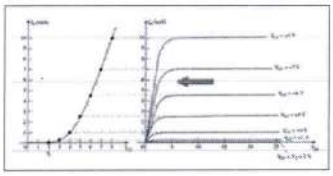


E-Type MOSFET Transfer Curve

To determine I_D given V_{GS}:

$$I_D = k(V_{GS} - V_T)^2$$

Where:
V_T = threshold voltage or voltage at which the MOSFET turns on



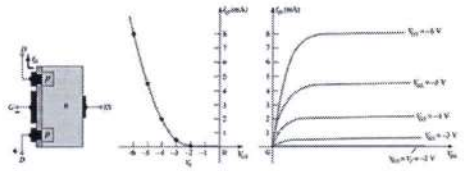
k, a constant, can be determined by using values at a specific point and the formula:

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

V_{DSsat} can be calculated by:

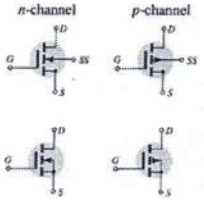
$$V_{Dsat} = V_{GS} - V_T$$

p-Channel E-Type MOSFETs



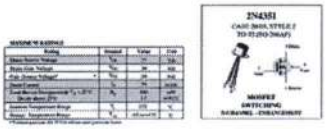
The *p*-channel enhancement-type MOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed.

MOSFET Symbols



Specification Sheet

Maximum Ratings



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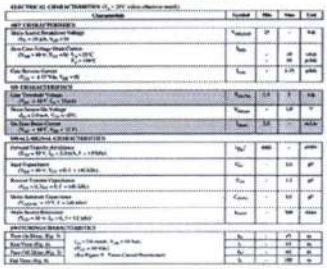
Specification Sheet

Electrical Characteristics



Handling MOSFETs

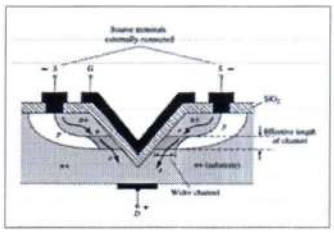
MOSFETs are very sensitive to static electricity. Because of the very thin SiO_2 layer between the external terminals and the layers of the device, any small electrical discharge can create an unwanted conduction.

Protection

- **Always transport in a static sensitive bag**
- **Always wear a static strap when handling MOSFETS**
- **Apply voltage limiting devices between the gate and source, such as back-to-back Zeners to limit any transient voltage.**

VMOS Devices

VMOS (vertical MOSFET) increases the surface area of the device.

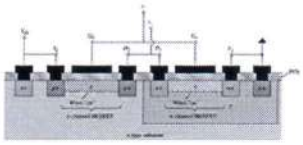


Advantages

- **VMOS devices handle higher currents by providing more surface area to dissipate the heat.**
- **VMOS devices also have faster switching times.**

CMOS Devices

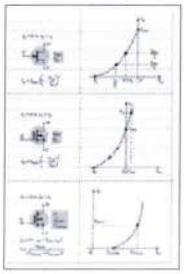
CMOS (complementary MOSFET) uses a *p*-channel and *n*-channel MOSFET; often on the same substrate as shown here.



Advantages

- **Useful in logic circuit designs**
- **Higher input impedance**
- **Faster switching speeds**
- **Lower operating power levels**

Summary Table



OUTLINE

- Field Effect Transistor (FET)
- Junction Field Effect Transistor (JFET)
- Construction of JFET
- Theory of Operation
- I-V Characteristic Curve
- Pinch off Voltage (V_P)
- Saturation Level
- Break Down Region
- Ohmic Region
- Cut off Voltage
- Advantages
- Disadvantages
- Application of JFET

INTRODUCTION

The ordinary or bipolar transistor has two main disadvantage.

- It has a low input impedance
- It has considerable noise level

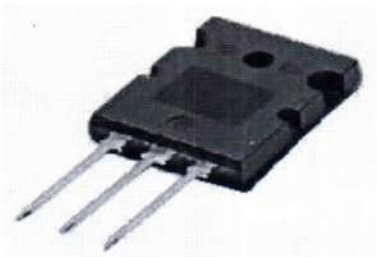
To overcome this problem Field effect transistor (FET) is introduced because of its:

- High input impedance
- Low noise level than ordinary transistor

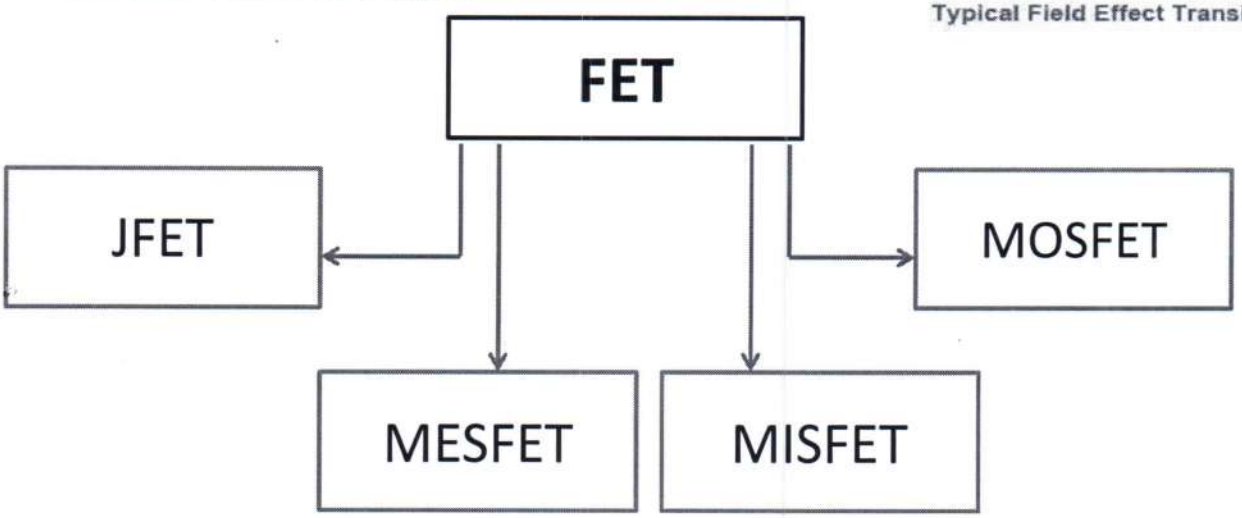
And Junction Field Effect Transistor (JFET) is a type of FET.

Field Effect Transistor (FET)

- FET is a voltage controled device.
- It consists of three terminal .
  - Gate
  - Source
  - Drain
- It is classified as four types.



Typical Field Effect Transistor



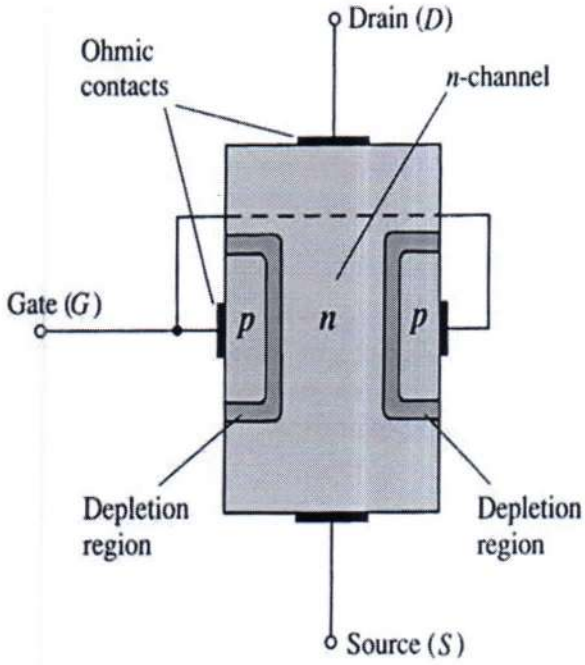
Construction of JFET

❑ **Source:** The terminal through which the majority carriers enter into the channel, is called the *source* terminal S .

❑ **Drain:** The terminal, through which the majority carriers leave from the channel, is called the *drain* terminal D .

❑ **Gate**: There are two internally connected heavily doped impurity regions to create two P-N junctions. These impurity regions are called the *gate* terminal G.

❑ **Channel**: The region between the source and drain, sandwiched between the two gates is called the *channel* .



Mid & Assignment Examination Question Papers with scheme and solutions (for problems)

ASSIGNMENT QUESTION PAPERS WITH SCHEME OF EVALUATION

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NARASARAOPET
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
II B.TECH I-SEMESTER ASSIGNMENT TEST-I, January -2021

SUBJECT: ELECTRONIC DEVICES AND CIRCUITS	DATE: 27-01-2021
DURATION: 30 MIN	MAX MARKS: 10

SCHEME OF EVALUATION

Q. No	Questions	Course Outcome (CO)	Knowledge Levels as Per Bloom's Taxonomy	Max. Marks
1	Identify the breakdown mechanisms in a diode, explain and compare them.	1	Applying (K3)	05
	Definition -1M Diagram -1M Any three differences-3M			
2	Utilize the energy band diagrams to explain the working and V-I characteristics of Tunnel diode.	1	Applying (K3)	05
	Diagram -1M Working -2M V-I characteristics -2M			
3	Make use of the circuit and necessary waveforms to explain the construction and operation of LED.	1	Applying (K3)	05
	Circuit -1M Wave forms -1M Explanation of construction and operation-3M			
4	Make use of the circuit and necessary waveforms to explain the operation of bridge rectifier.	1	Applying (K3)	05
	Circuit -1M Wave forms -1M Explanation of operation -3M			
5	Develop the equations for rectification efficiency and ripple factor for the following. (a)Half wave rectifier (b) Full wave rectifier	1	Applying (K3)	05
	Equation of efficiency(HWR) -1.5M Ripple factor(HWR) -1M Equation of efficiency(HWR) -1.5M Ripple factor(HWR) -1M			
6	Develop the equation for ripple factor of full wave rectifier with capacitor filter.	1	Applying (K3)	05
	Equation for ripple factor -5M			

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
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SUBJECT: ELECTRONIC DEVICES AND CIRCUITS	DATE: 27-01-2021
DURATION: 30 MIN	MAX MARKS: 10

Q. No	Questions	Course Outcome (CO)	Knowledge Levels as Per Bloom's Taxonomy	Max. Marks
1	Identify the breakdown mechanisms in a diode, explain and compare them.	1	Applying (K3)	05
2	Utilize the energy band diagrams to explain the working and V-I characteristics of Tunnel diode.	1	Applying (K3)	05
3	Make use of the circuit and necessary waveforms to explain the construction and operation of LED.	1	Applying (K3)	05
4	Make use of the circuit and necessary waveforms to explain the operation of bridge rectifier.	1	Applying (K3)	05
5	Develop the equations for rectification efficiency and ripple factor for the following. (a)Half wave rectifier (b) Full wave rectifier	1	Applying (K3)	05
6	Develop the equation for ripple factor of full wave rectifier with capacitor filter.	1	Applying (K3)	05

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
II B.TECH I-SEMESTER ASSIGNMENT TEST-III, February -2021

SUBJECT: ELECTRONIC DEVICES AND CIRCUITS	DATE: 16-02-2021
DURATION: 30 MIN	MAX MARKS: 10

Q. No	Questions	Course Outcome (CO)	Knowledge Levels as Per Bloom's Taxonomy	Marks
1	a) Develop the relation among **α , β and γ** b) Demonstrate the working of PNP transistor with neat diagram.	1	Understanding (K2)	05
2	Compare and contrast the transistor characteristics used in defining regions of operation of a transistor connected in CB configuration.	2	Analyze (K4)	05
3	Illustrate and explain input and output characteristics of a NPN BJT connected in CE configuration with neat graphs.	1	Applying (K3)	05
4	A transistor is connected in CE configuration, in which collector supply is 8v and voltage drop across resistance (Rc) connected to the collected circuit is 0.5v. The value of Rc = 800Ω. If $\infty = 0.96$ i)Collector -Emitter Voltage ii) Base Current	1	Applying (K3)	05
5	Make use of circuit and necessary waveforms to explain the construction and operation of n-channel FET.	1	Applying (K3)	05
6	Utilize the Drain and transfer characteristics in order to explain the functionalities of n-channel JFET.	1	Applying (K3)	05

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
II B.TECH I-SEMESTER ASSIGNMENT TEST-III, February -2021

SUBJECT: ELECTRONIC DEVICES AND CIRCUITS	DATE: 16-02-2021
DURATION: 30 MIN	MAX MARKS: 10

SCHEME OF EVALUATION

Q. No	Questions	Course Outcome (CO)	Knowledge Levels as Per Bloom's Taxonomy	Marks
1	a) Develop the relation among **α , β and γ** b) Demonstrate the working of PNP transistor with neat diagram.	1	Understanding (K2)	05
	a.equation for relation of parameters -2M b.Diagram -1M working -2M			
2	Compare and contrast the transistor characteristics used in defining regions of operation of a transistor connected in CB configuration.	2	Analyze (K4)	05
	Diagram of CB -2M Operation of transistor -3M			
3	Illustrate and explain input and output characteristics of a NPN BJT connected in CE configuration with neat graphs.	1	Applying (K3)	05
	Diagram of CB -2M Input characteristics -1.5M Out put characteristics -1.5M			
4	A transistor is connected in CE configuration, in which collector supply is 8v and voltage drop across resistance (Rc) connected to the collected circuit is 0.5v. The value of Rc = 800Ω. If $\infty = 0.96$ i)Collector –Emitter Voltage ii) Base Current	1	Applying (K3)	05
	1.Collector-Emitter voltage answer-2.5M 2.Base current value -2.5M			
5	Make use of circuit and necessary waveforms to explain the construction and operation of n-channel FET.	1	Applying (K3)	05
	Circuit diagram -1M Wave forms -1M Explanation of construction and operation -3M			
6	Utilize the Drain and transfer characteristics in order to explain the functionalities of n-channel JFET.	1	Applying (K3)	05
	Wave forms -2M Explanation of n-channel JFET -3M			

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II B.TECH I-SEMESTER ASSIGNMENT TEST-IV, MARCH -2021

SUBJECT: ELECTRONIC DEVICES AND CIRCUITS	**DATE: 2-03-2021**
DURATION: 30 MIN	**MAX MARKS: 10**

Q. No	Questions	Course Outcome (CO)	Knowledge Levels as Per Bloom's Taxonomy	Max
1	Make use of circuit diagram to explain the Collector to base bias circuit.	4	Applying (K3)	05
2	Make use of circuit diagram to explain the Fixed bias circuit.	4	Applying (K3)	05
3	Identify the different types of MOSFETs and briefly explain the construction and operation of Enhancement mode MOSFET.	5	Applying (K3)	05
4	Make use of circuit diagram to explain the construction and operation of Depletion mode MOSFET.	5	Applying (K3)	05
5	Make use of circuit diagram to explain the construction and operation of SCR.	5	Applying (K3)	05
6	Make use of circuit diagram to explain the construction and operation of UJT.	5	Applying (K3)	05

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II B.TECH I-SEMESTER ASSIGNMENT TEST-IV, MARCH -2021

SUBJECT: ELECTRONIC DEVICES AND CIRCUITS	DATE: 2-03-2021
DURATION: 30 MIN	MAX MARKS: 10

SCHEME OF EVALUATION

Q. No	Questions	Course Outcome (CO)	Knowledge Levels as Per Bloom's Taxonomy	Max
1	Make use of circuit diagram to explain the Collector to base bias circuit.	4	Applying (K3)	05
	Circuit diagram -2M Explain the Collector to base bias circuit.-3M			
2	Make use of circuit diagram to explain the Fixed bias circuit.	4	Applying (K3)	05
	Circuit diagram -2M Explain the Fixed bias circuit. -3M			
3	Identify the different types of MOSFETs and briefly explain the construction and operation of Enhancement mode MOSFET.	5	Applying (K3)	05
	Different types of MOSFETs -2M Explain of the construction -1.5M Explanation of operation -1.5M			
4	Make use of circuit diagram to explain the construction and operation of Depletion mode MOSFET.	5	Applying (K3)	05
	Circuit diagram -2M Explain of the construction -1.5M Explanation of operation -1.5M			
5	Make use of circuit diagram to explain the construction and operation of SCR.	5	Applying (K3)	05
	Circuit diagram -2M Explaination of the construction -1.5M Explanation of operation -1.5M			
6	Make use of circuit diagram to explain the construction and operation of SCR.	5	Applying (K3)	05
	Circuit diagram -2M Explain of the construction -1.5M Explanation of operation -1.5M			

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Year 02 Semester 2 Sec D Test No 03

Sub LDC Date 16/05/21

Name CH.V.Prasanth

HALL TICKET NO.

1	7	U	7	1	A	0	U	I	7

MARKS 06 (Tens 0, Ones 6) Marks in words Zero Six

Signature of the Principal — Signature of the Examiner - I — Signature of the Examiner - II

1.) photo transistor:

the photo transistor is also called as photodiode. It is a much more sensitive semiconductor photo device that than the p-N photo diode. the photo transistor is usually connected in a common emitter configuration with the biased open, and the radiation is concentrated on the region near the collector junction (J_c) as shown in Fig 1(a).

the operation of the device can be understood if we recogine that the junction J_e is slightly forward biased and the junction J_c is reverse biased. i.e the transis. -tor is biased in the active region.

the collector current is given by

$$I_c = (\beta+1) I_{co} \text{ with } I_B = 0$$

Fig 1(a): photo transistor.

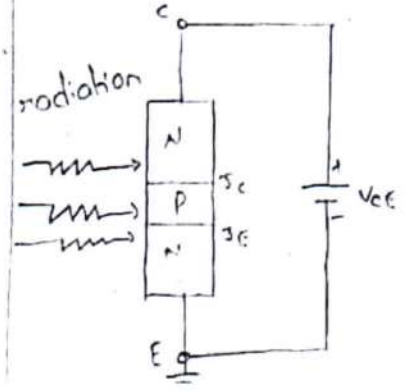
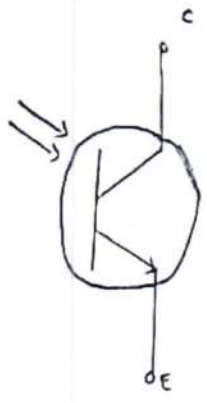
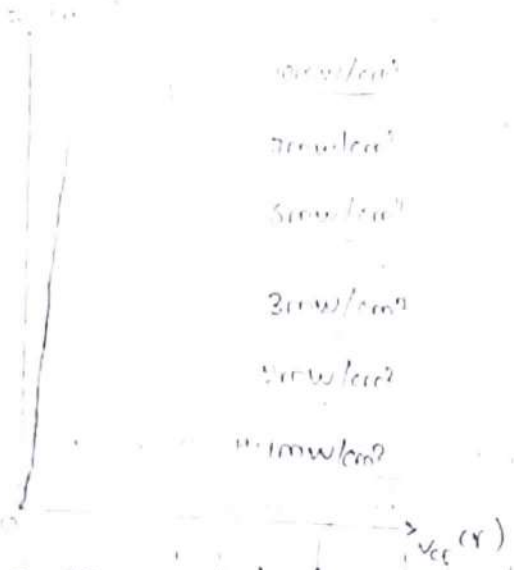


Fig 1(b): circuit Symbol.

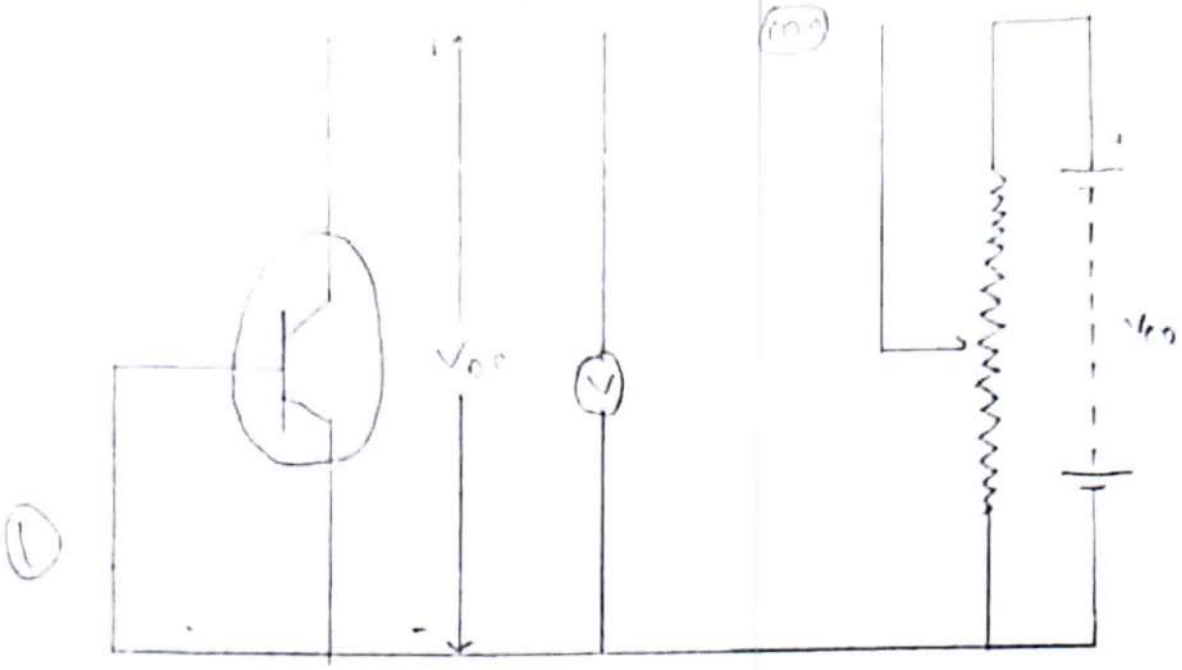


shown in Fig 6(b).



The above Figure indicates the output characteristics of an photo transistor.

Typically voltage-amphere characteristics are shown in the above figure for a ~~Pn~~ n-Pn (~~planes~~) planar photo transistor for ~~diff~~ different values of illumination intensities.


(1)
V_{CE}
V
(100)
V_{CC}

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Year II Semester I Sec D Test No 1)

Sub EDC Date 16/02/21

Name Ch. Bhanu Prakash

HALL TICKET NO									
1	9	4	7	1	A	0	4	J	4

MARKS 10 | 1 | Marks in words Ten | One

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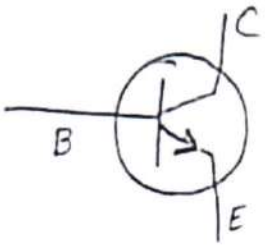
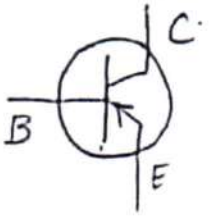
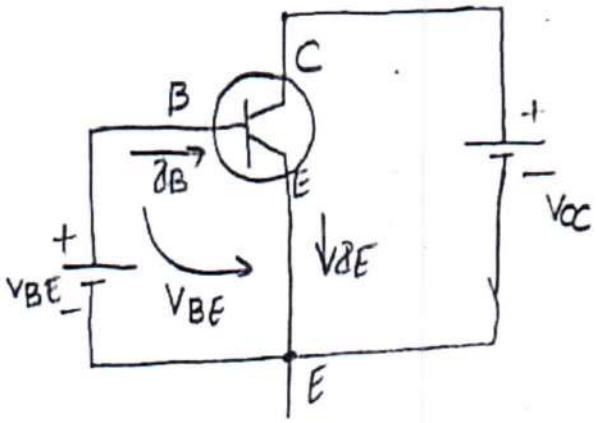
2) In common emitter configuration common base is emitter



(1) P-N-P



N-P-N



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Year II Semester I Sec D Test No 3

Sub EDC Date 16-02-21

Name V. Arun Kumar

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1	8	4	7	1	A	0	4	M	0

Tens Ones

MARKS 10 Marks in words ONE ZERO

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(1) In CB configuration the amplification factor is $\alpha = \frac{\Delta I_C}{\Delta I_E}$ - (1)

In CE configuration the amplification factor is $\beta = \frac{\Delta I_C}{\Delta I_B}$ - (2)

In CC configuration the amplification factor is $\gamma = \frac{\Delta I_B}{\Delta I_E}$ - (3)

The relationship between α and β :-

We know that

$I_C = I_E + I_B$

By the defination

$\alpha = \frac{\Delta I_C}{\Delta I_E}$

$I_C - I_E = I_B$

$I_E(1-\alpha) = I_B$.

Dividing with I_C on b.s

$\frac{I_E}{I_C}(1-\alpha) = \frac{I_B}{I_C}$

$\frac{1}{\beta}(1-\alpha) = \frac{1}{\beta}$

In CC configuration input is I_B and the output is I_E

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

We know that

$$I_C = I_B + I_E$$

$$I_E = I_C - I_B.$$

$$\gamma = \frac{\Delta I_E}{\Delta I_C - \Delta I_B}$$

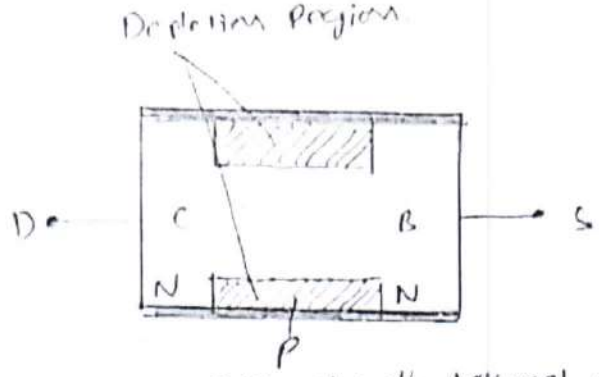
dividing with I_E numerator and denominator on R.H.S side.

$$\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_C}{\Delta I_E} - \frac{\Delta I_B}{\Delta I_E}} \qquad \gamma = \frac{\alpha}{\beta + 1}$$

$$\gamma = \frac{1}{1 - \alpha} \quad (or) \quad \boxed{\gamma = \frac{1}{\beta + 1}}$$

3	Build the relation between Alpha, Beta and Gama parameters of transistor	3	Applying (K3)	05
5	Make use of circuit diagram to explain the construction and operation of n-channel JFET	1	Applying (K3)	05

(a)



construction of n-channel JFET

The N-channel is made of silicon, ohmic of two ends of the terminal.

Source :- It is connected to the negitive pole of the battery. The minority of carriers are leave enter through the n-channel in the bar

Drain :- It is connected to the positive pole of the battery and the maiority of carriers are leave through the n-channel in the bar.

Gate :- The BC region between the two depletion regions connected to each other is called as gate.

When $V_{DS} \neq 0$ and

⇒ Operations of the n-channel :-

* when $V_{DS} = 0$ and $V_{GS} = 0$:- In this condition, the It is in the reverse biased. no voltage is applied in this conditions.

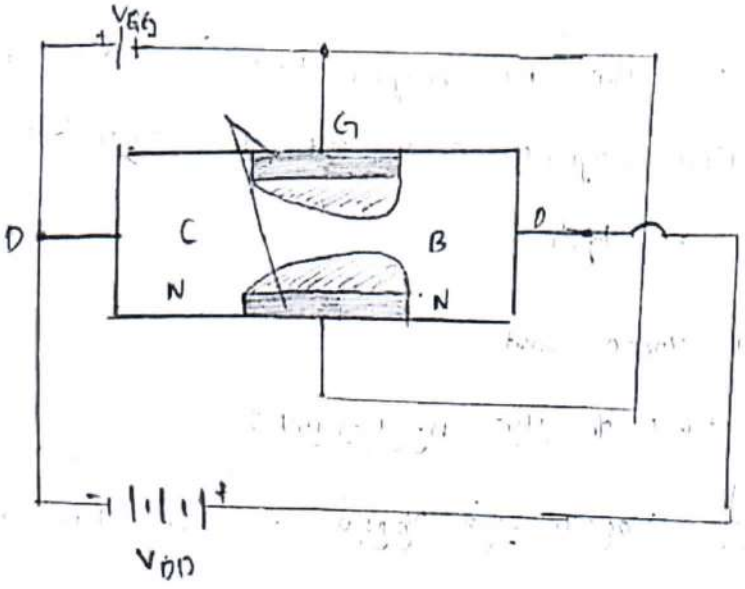
condition the circuit is in the forward biased and it acts as the forward biased the when the depletion region is increased. And V_{DS} is decreasing exponentially from zero the current flows from the Ground to source.

* when $V_{DS} = 0$ and V_{GD} is increasing :- In this condition the carriers are move from the source to Drain. source and the Drain with respect V_{GD} is increasing exponentially from the zero The magnitude of the current following the these conditions.

(1) it is having the majority of carriers in the n-channel

(2) And it having the length 'L'

(3) The area of A in B channel.

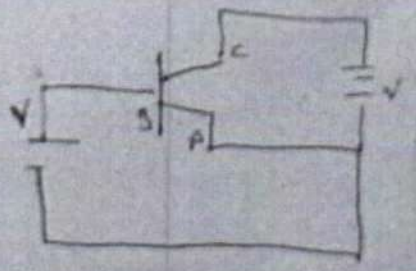


Under applied bias n-channel JFET

2020 (A)

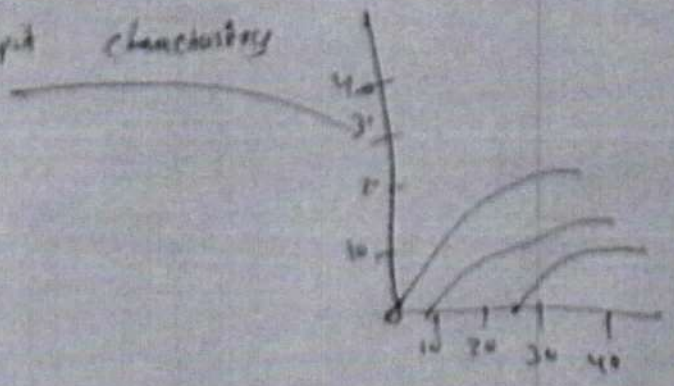
Explain the input and output characteristics of CE (common emitter) configuration

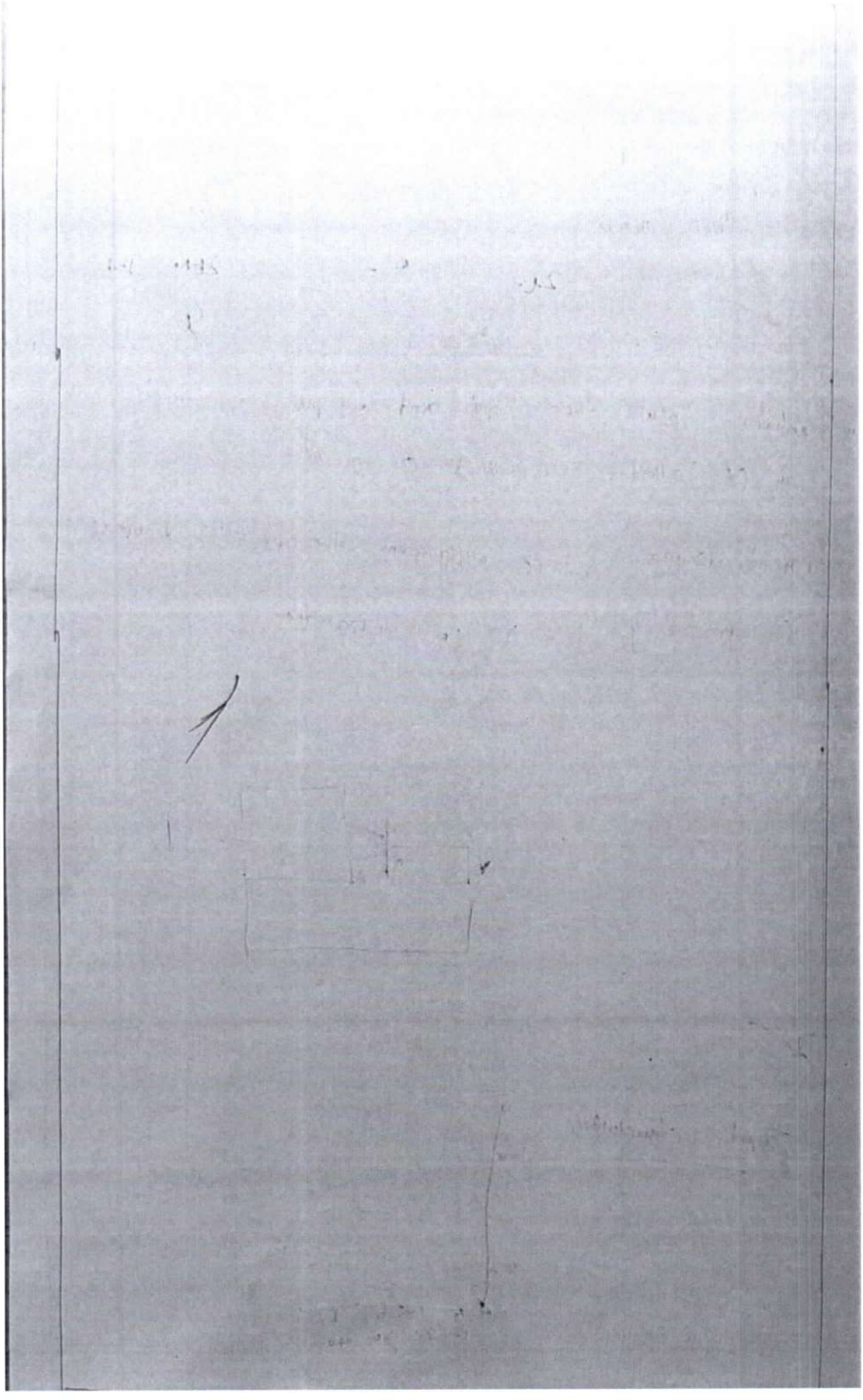
Circuit diagram for CE configuration the emitter terminal is grounded for CE configuration



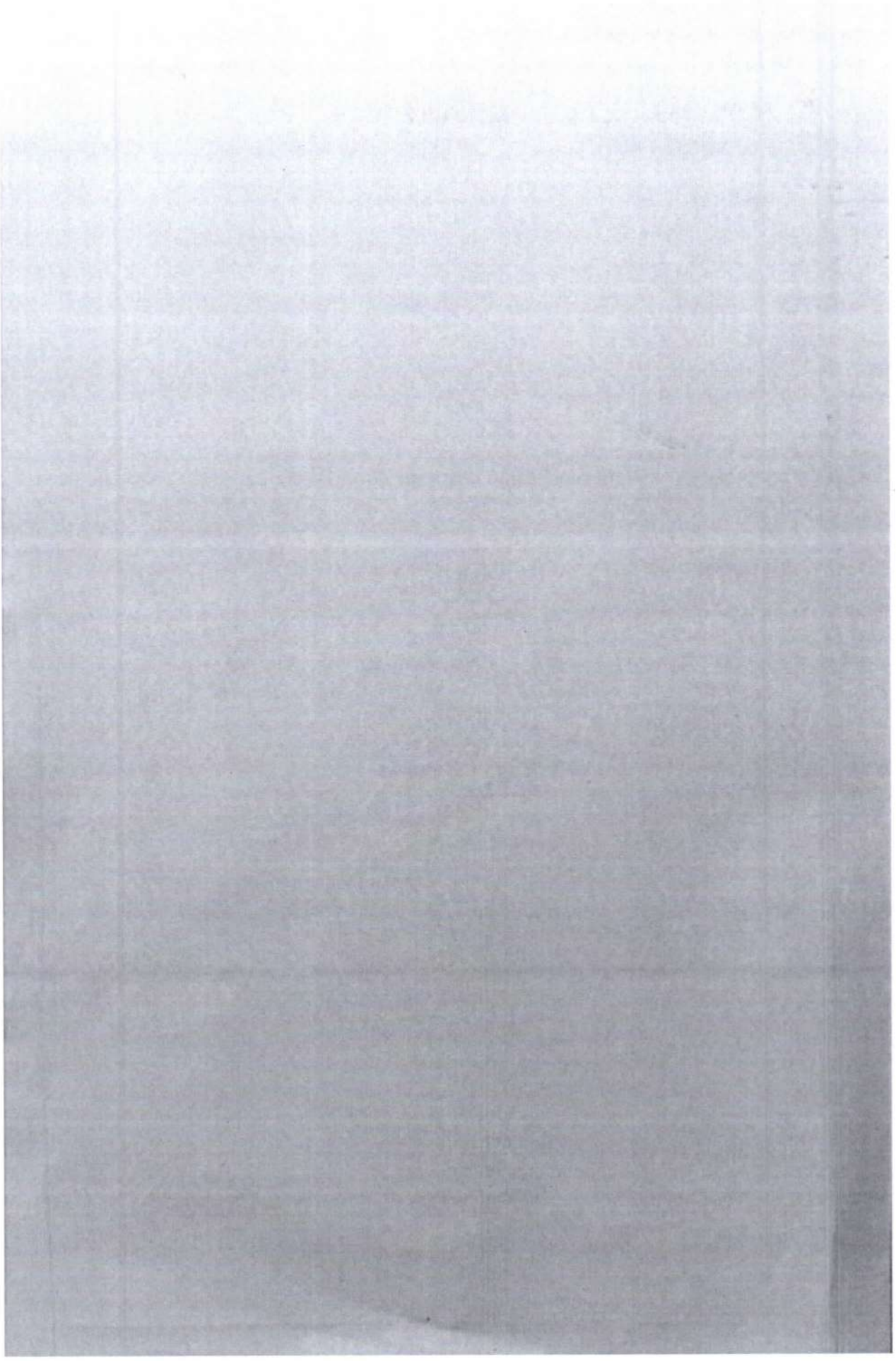
2)

Input characteristics





- the circuit and necessary waveforms to explain it's operation in drain and transfer characteristics of JFET



ASSIGNMENT TEST ANSWER BOOK

2020 (A) 68000

HALL TICKET NO: 1 9 4 7 1 A 0 4 F 5

Year II Semester I Sec C Test No 3

Sub Electronic devices & Circuits Date 16-2-2021

Name K. Uday Krishna Chaitanya

MARKS 10 (Tens 1, Ones 0) Marks in words ONE ZERO

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1 Ans)

Relationship between Alpha, Beta and Gama Parameters:

(i) Relationship between α and β:

we know that $\alpha = \frac{I_C}{I_E}$, $\beta = \frac{I_C}{I_B}$

we have $I_E = I_B + I_C$

$\Rightarrow I_B = I_E - I_C$

Substitute I_B in β, then

$\beta = \frac{I_C}{I_E - I_C}$ divide numerator and denominator with I_E

$= \frac{I_C/I_E}{\frac{I_E - I_C}{I_E}} = \frac{I_C/I_E}{1 - \frac{I_C}{I_E}}$ $\left(\because \alpha = \frac{I_C}{I_E}\right)$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

divide with $1+\beta$ on both sides

$$\frac{\beta}{1+\beta} = \frac{\frac{\alpha}{1-\alpha}}{1+\beta} = \frac{\frac{\alpha}{1-\alpha}}{1+\frac{\alpha}{1-\alpha}} = \frac{\frac{\alpha}{1-\alpha}}{\frac{1}{1-\alpha}}$$

$\Rightarrow$ $$\boxed{\frac{\beta}{1+\beta} = \alpha}$$

We have, $I_E = I_B + I_C$

$I_B = I_E - I_C$, Sub I_B in γ, then

$$\gamma = \frac{I_E}{I_E - I_C} = \frac{1}{1 - \frac{I_C}{I_E}} = \frac{1}{1-\alpha}$$

$$\therefore \gamma = \frac{1}{1-\alpha}$$

(iii) Relation between β and γ :

We know that, $\beta = \frac{\alpha}{1-\alpha}$

add '+1' on both sides, then

$$1+\beta = \frac{\alpha}{1-\alpha} + 1$$

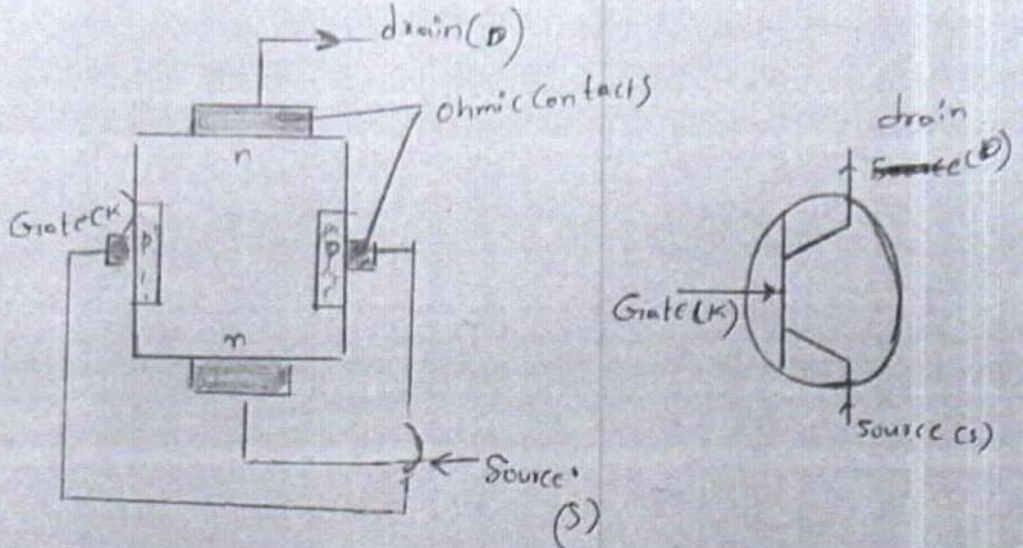
$$1+\beta = \frac{1}{1-\alpha} = \gamma$$

$$\Rightarrow \gamma = 1+\beta$$

$$\beta = \frac{\alpha}{1-\alpha} = \alpha \frac{1}{1-\alpha} = \alpha\gamma$$

i) Circuit diagram :-

n-channel JFET :-



Construction :-

A bar of extrinsic Semiconductor n type material with two ends, two ohmic Contacts which are made used by drain and Source terminals. A Heavily doped electrodes of P type form P-n Junctions on the base of terminals. The thin layer between two P-gates is Known as Channel. The channel is called as n-channel of JFET

The elements enter in to terminals through Source and leave through drain. The heavily doped Electrodes which are taken are Known as gates The electrodes all are Connected together only one terminal which is taken Out is Known as

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B.Tech / M.Tech / MBA / MCA / B Tech (Br.) ECE 2020 (A) 35974

Year 02 Semester 01 Sec C Test No 03

Sub EDC Date 16/02/2021

Name B. Chiranjeevi

HALL TICKET NO: 1 9 4 7 1 A 0 4 C 7

MARKS: Tens 0, Ones 5 — Marks in words: ZERO FIVE

5 X 0

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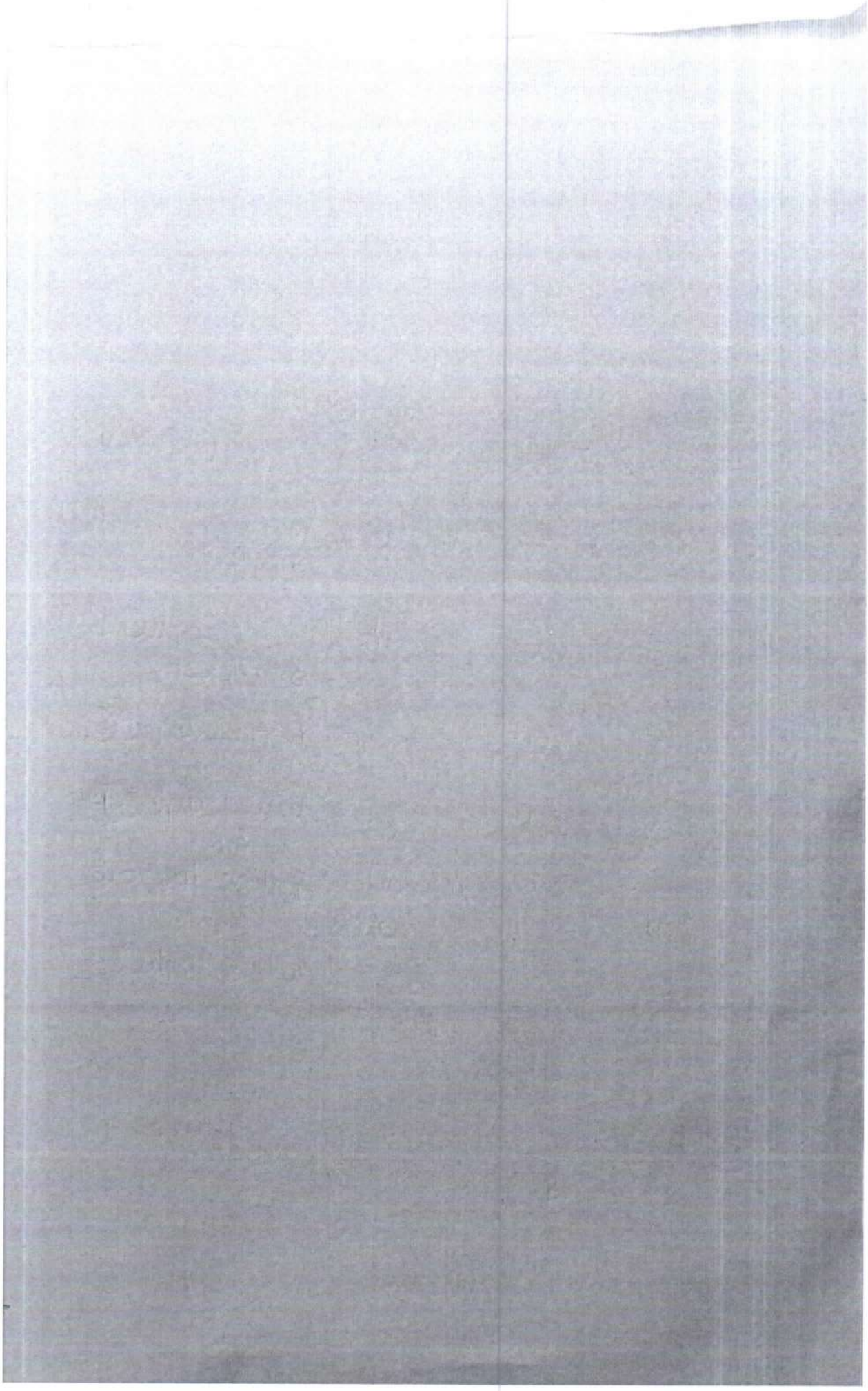
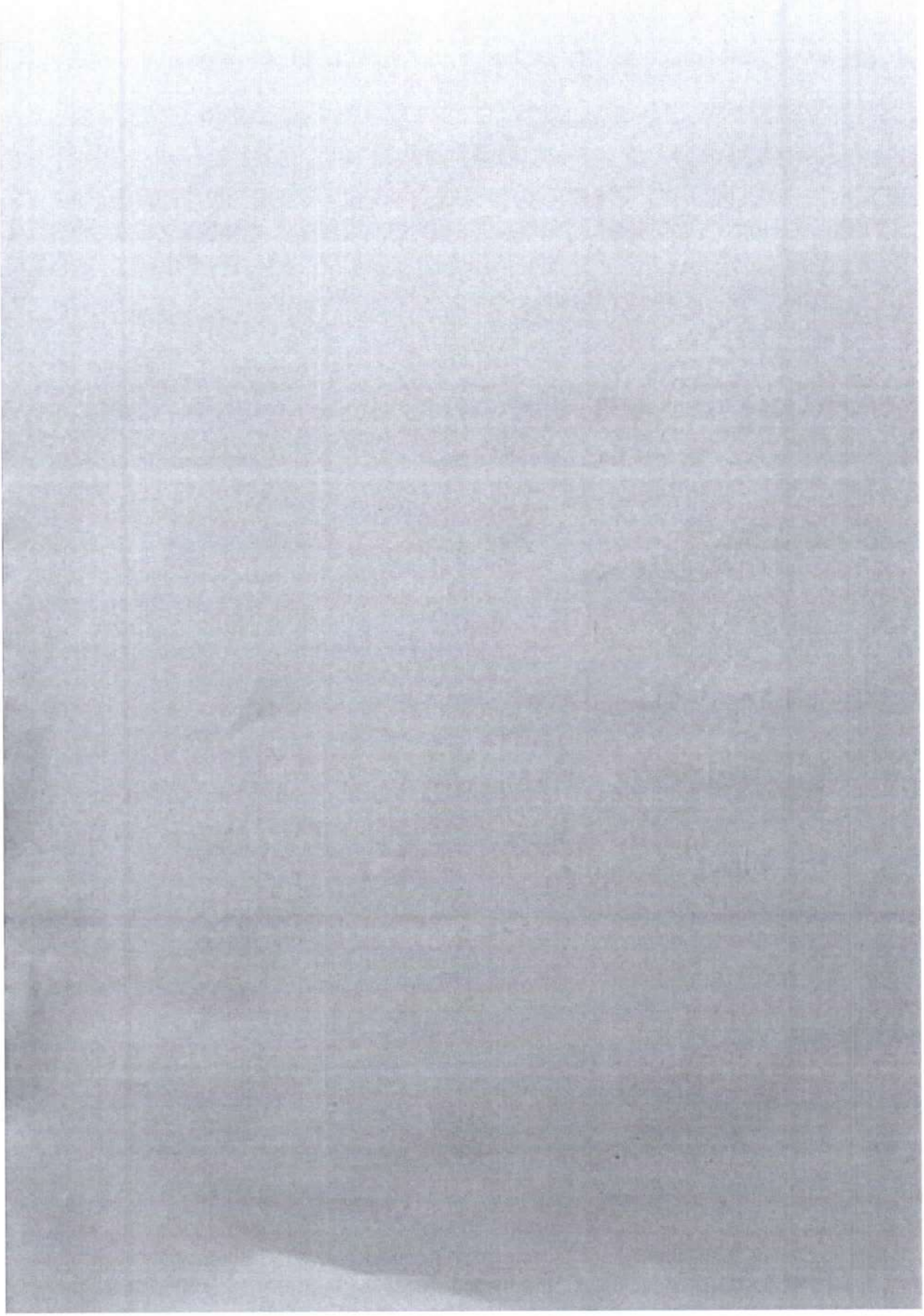
(3)

Parameter	Common base	Common emitter	Common Collector
(1) Input resistance	very low	low	high
(2) Output resistance	very high	high	low
(3) Input Current	I_E	I_B	I_B
(4) Output Current	I_C	I_C	I_E
(5) Input voltage	Emitter and base	Base and emitter	Base and collector
(6) Output voltage	Collector and base	Collector and emitter	Emitter and collector
(7) Current Parameter.	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\eta = \frac{I_E}{I_B}$

5.





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ASSIGNMENT TEST ANSWER BOOK

B.Tech. / M.Tech. / M.B.A. / M.C.A. / B.Tech (Br.) ECE 2020 (A) 72515

Year II Semester I Sec. C Test No.

Sub EDC Date 27/01/21

Name E. Srinivas

HALL TICKET NO.

2	0	4	7	5	A	0	4	0	5

Tens Ones

MARKS Marks in words

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(1) a) Breakdown mechanism in a diode. - S.t.2 = (7)

* The Breakdown mechanism is two types

i. Avalachi Breakdown

ii. Zenar Breakdown

* The Breakdown mechanism is in Reverse bias condition.

* If the Breakdown voltage is increases. then the covalent Bonds are broken.

* The Reverse Saturation current is Because of Minority charge carriers electron in p type and holes in n type

* If the reverse Saturation current is increasy it reaches certain point then it raises rapidly Because of Breakdown of junction.

* Breakdown mechanisms are two types Avalanchi Breakdown and Zenar Breakdown

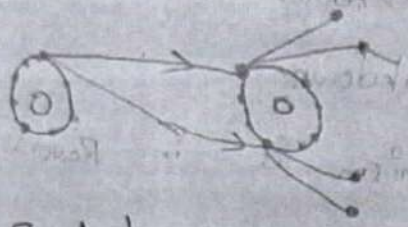
* It is the breakdown because of breaking of covalent bonds.

* In Reverse bias condition the minority current flows in a diode of minority charge carrier of electron in p-type and holes in n-type is called reverse saturation current.

* In this the depletion region is large.

* If the increase in reverse saturation current it reaches certain point then breaks the junction

* This is called "Avalanche Breakdown".



II. Zener Breakdown.

* In Reverse Bias condition the minority current flows because of minority charge carriers present in a diode.

* In this the depletion layer width is small so the electrons jumps the junction easily and so large current flows through it.

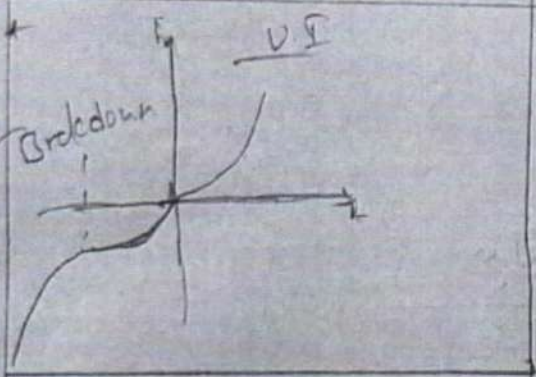
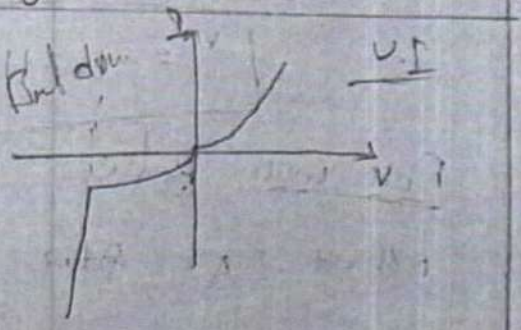
* This is called "Zener Breakdown".

* The VI characteristics of Zener Breakdown is shown.

* It is used for the heavily doped diodes

Q. No.	Question	Course Outcomes (CO)	Knowledge Levels as Per Bloom's Taxonomy	Marks
1	Identify the breakdown mechanisms in a diode, explain and compare them	1	Applying (K3)	05
2	Develop the equations for rectification efficiency and ripple factor for the following (a)Half wave rectifier (b) Full wave rectifier.	1	Applying (K3)	05

Comparision between Avalanche & Zener Breakdown

Avalanche	Zener
* due to Breakdown of covalent bonds due to collision of electrons in a diode	* Breakdown of covalent bond due to electric field of the large current flows in a diode
* Temperature coefficient is positive	* Temper coeff is negative
	
* used in lightly doped diode	* used in heavily doped diode

(2) Half wave Rectifier:-

Rectification Efficiency:-

ratio of $\eta = \frac{P_{dc}}{P_{ac}} = \frac{\frac{I_m^2}{2} R_L}{\frac{I_m^2}{\pi^2}(R_f + R_L)}$

$\frac{4}{\pi^2}\left[1 - \frac{R_f + R_s}{R_L}\right]$

$R_f + R_s \ll R_L$ we neglate

$= 4 \cdot 0.4 \text{DB}$

$= 0.4 \text{DB}$

$\eta \% = 40.8$

Ripple Factor

$$\gamma = \frac{I_{a1}}{I_{d1}}$$

$$= \frac{I_{rms} - I_d}{I_{d1}}$$

$$= \sqrt{\frac{\pi^2}{4}}$$

$$\gamma = 1.211$$

Full wave Rectifier

Efficiency $\eta = \frac{I_{m1}}{\frac{I_m}{2}}$

$\eta = 81.2$

Ripple factor:

$\gamma = 48\%$

NEC

ASSIGNMENT TEST ANSWER BOOK

B-tech ECE 2020(A) 72443

Year 2 Sem 1 Sec C Series 1

Sub Electric devices & circuits Date 27/01/2021

Name V. Gauthami

HALL TICKET NO: 1 9 U 7 1 A 0 U H 9

MARKS: Tens Ones

Marks in words

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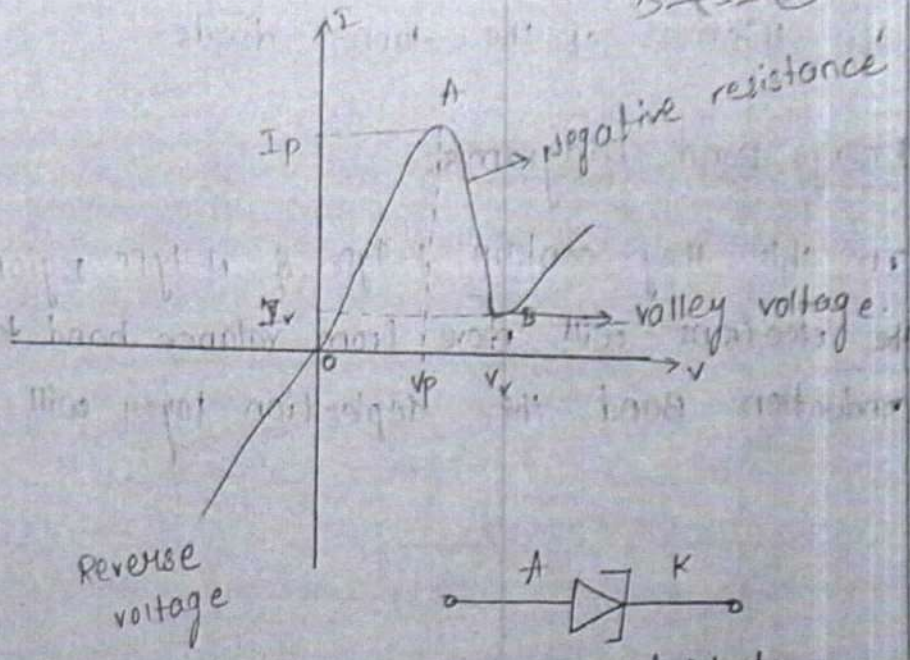
(1) V-I characteristics of Tunnel diode:- 5+5=(10)



Tunnel Diode.

* In forward Bias condicition as the voltage increases the forward current also increases quickly.
* The forward current reaches a peak value Ip with the voltage Vp
* Again if the voltage increases the current decreases from the peak value.
* The peak value as point A & B the between

the negative resistance region will be takes place.

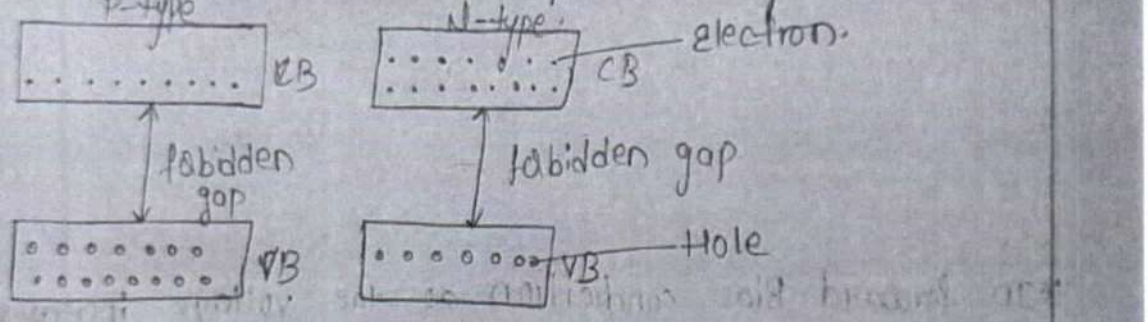
* the point B is known as valley current or valley voltage.

* Again if we increase the voltage again it raises from point B.

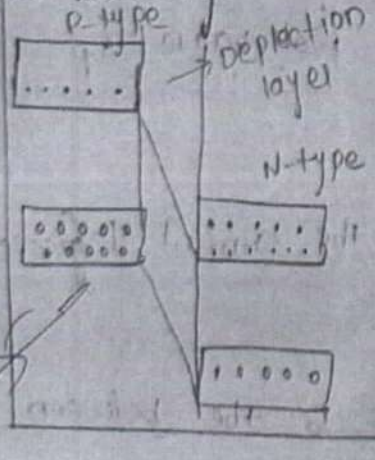
* In reverse voltage it is very different due to the thickness of the tunnel diode.

Energy Band Diagrams:-

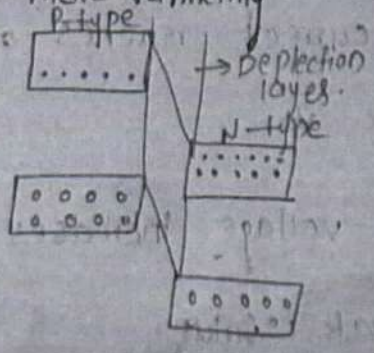
In this they contain P-type & N-type regions the electrons will move from valance band to the conduction Band the depletion layer will form.



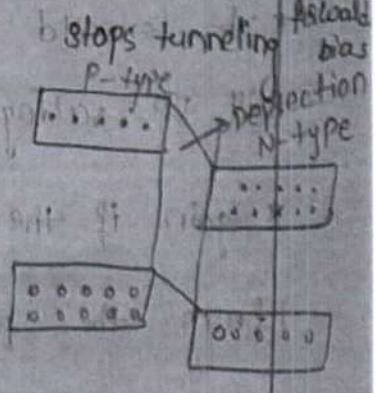
condition(i):-
No forward bias
No tunnelling



condition(ii):-
Small forward bias
more tunneling

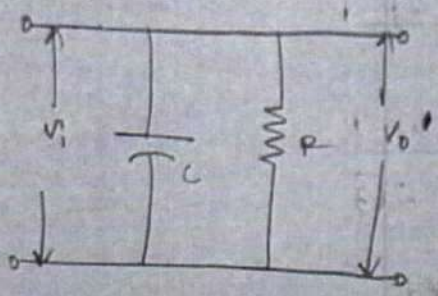


condition(iii):-
More increase in forward bias stops tunneling



Capacitor filter:

* It allows the ac current and stops the dc current is called capacitor filter.
* The operation of capacitor filter is to stop the / short the ripple.
* It leaves the dc to appear as output.



The charge aquired = $V_{r\,p-p} \times C$ ⟶ (1)

The charge lost = $V_{dc} \times T_2$ ⟶ (2)

from eqn (1) & (2)

In capacitor filter the charge aquired is equal to the charge lost

$$V_{r\,p-p} \times C = V_{dc} \times T_2$$

If the capacitor filter is more than the T_2 will becomes half of the time.

$$T_2 = T/2$$

$$= \frac{1}{2f}$$

Substituting in above eqn

$$V_{r\,p-p} \times C = \frac{V_{dc}}{2f}$$

$$\boxed{V_{r\,p-p} = \frac{V_{dc}}{2fc}}$$

We know, $V_{r\,rms} = \frac{V_{r\,p-p}}{2\sqrt{3}}$

$$V_{r\,p-p} = \frac{V_{dc}}{2fc(2\sqrt{3})}$$

$$V_{r\,p-p} = \frac{V_{dc}}{4\sqrt{3}fc}$$

$$\boxed{\frac{V_{r\,p-p}}{V_{dc}} = \frac{1}{4\sqrt{3}fc}}$$

Ripple factor for capacitor filter is $\boxed{\frac{V_{r\,p-p}}{V_{dc}} = \frac{1}{4\sqrt{3}fc}}$.

The increase or decrease in the ripple factor is with the change in C or f

B.Tech M.Tech MBA MCA : B.Tech (Regular) E.C.E 2020 (A) 72133

Year II Semester I Sec C Test No 02

Sub E.D.C Date 27/01/2022

Name Gopi.S

HALL TICKET NO.

1	9	4	7	1	A	0	4	6	8

Tens Ones

MARKS Marks in words

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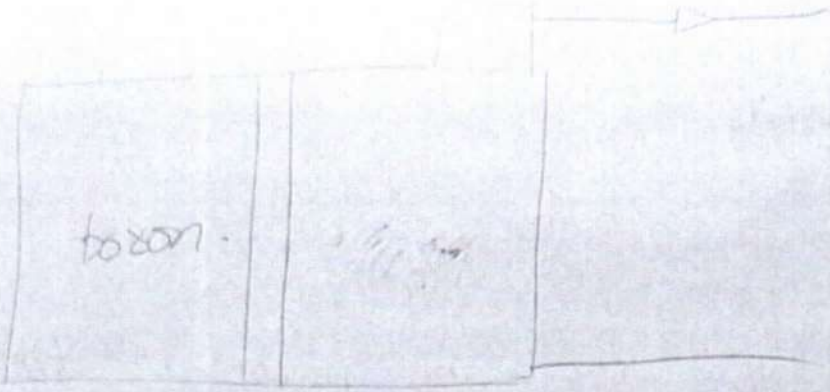
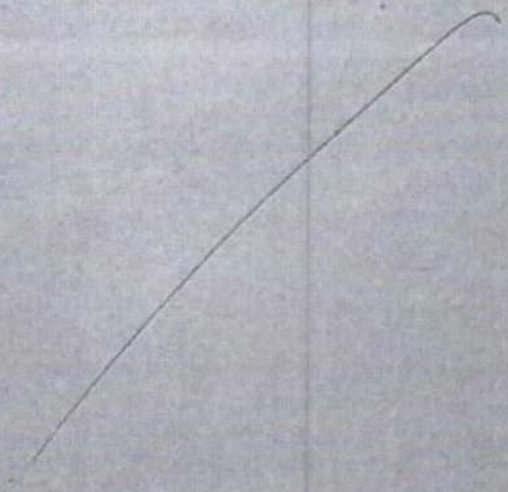
Then the LED it's necessary wave forms to construction & operation 1+0=(1) to connect a circuit of the boron of then it's passing through the necessary of anode to connecting with it's to Negitive circuit and of it's mainly to conkun's the powerfully reaction of it's connectivity of ten we taken the form of the for it's waveforms and the to many circuit connecting with the highly ~~continue~~ to the Blime to the possitive cell and connect it's possperouy the it's Blinking to the LED. It's the mainly to the conecting to the mainly to prove the it's self.

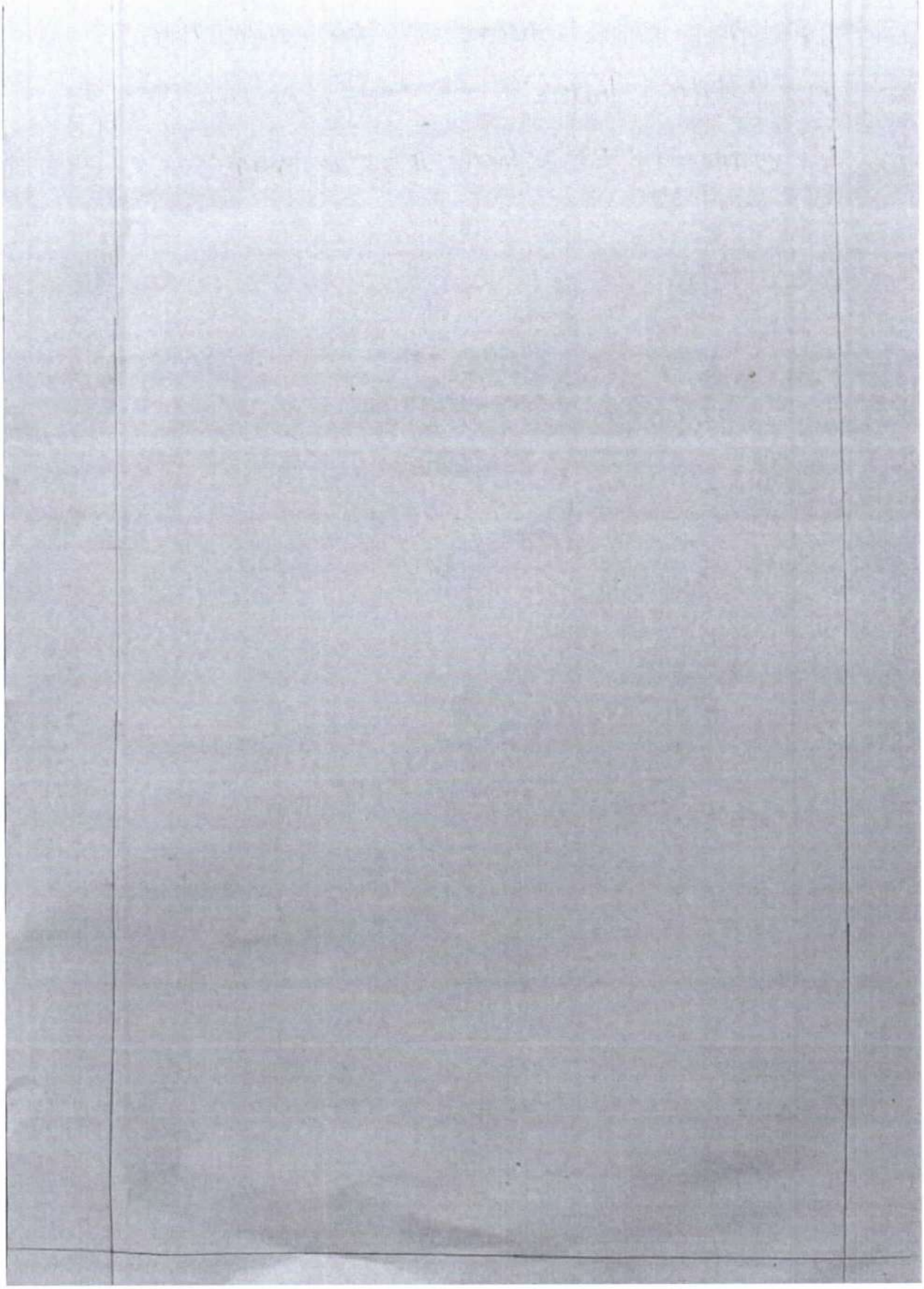
(1)


toxon.

1	Make use of the circuit and necessary instruments to explain the construction and operation of LED.	1	Applying (K3)	05
2	Develop the equations for rectification efficiency and ripple factor for the following (a) Half wave rectifier (b) Full wave rectifier	1	Applying (K3)	05

Then the ripple factor of the efficiency &
it's ripple factor of the rectification of
the main function then it's a very





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ASSIGNMENT TEST ANSWER BOOK

2020 (A) 8428

B.Tech / M.Tech / M.B.A / M.C.A / B.Tech (Br.) ECE

Year II Semester II Sec D Test No 1

Sub EDC Date 19/1/2021

HALL TICKET NO: 19 07 1A 04 H5

Name: Shaik Nagoor Meeravali

MARKS 04 Marks in words Four

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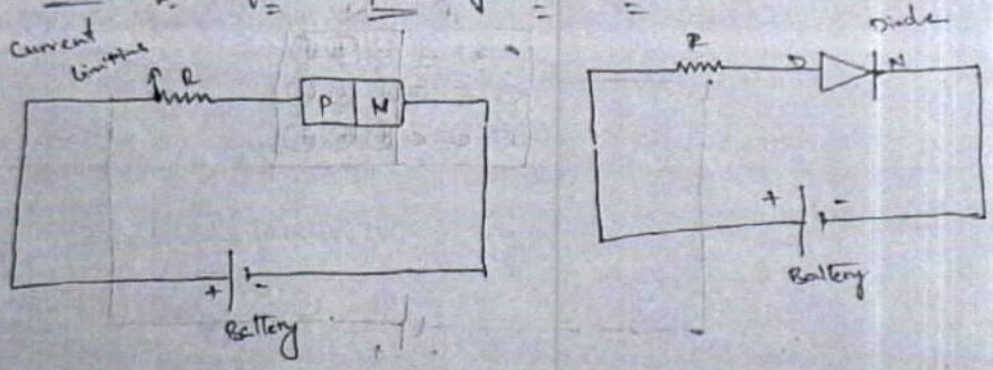
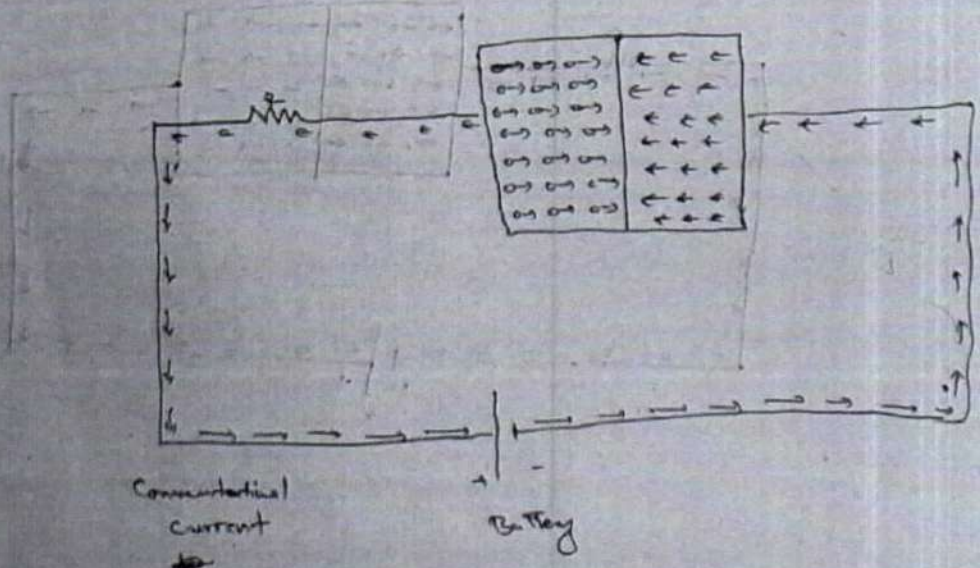
2+2=(4)

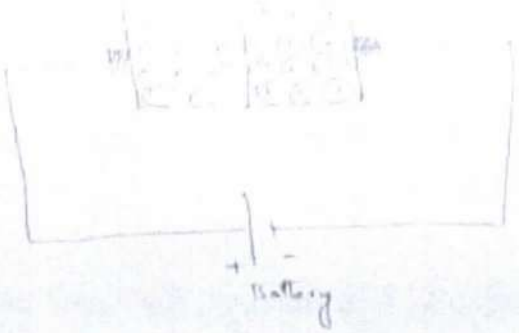
1A) providing an external DC voltage to the electrical circuit is called Bias.

Forward Bias of a P-N Junction Diode:-

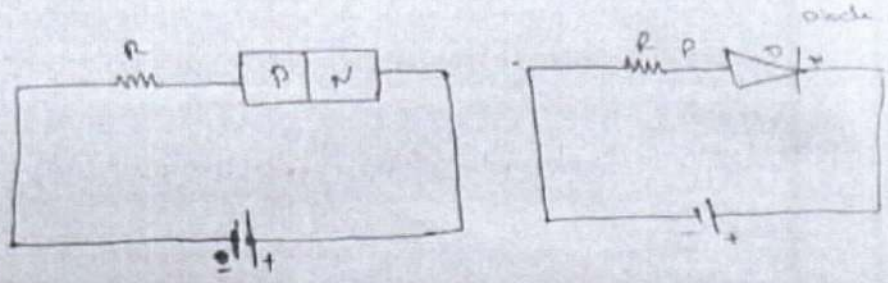


Operation on Forward Bias P-N Junction diode:-

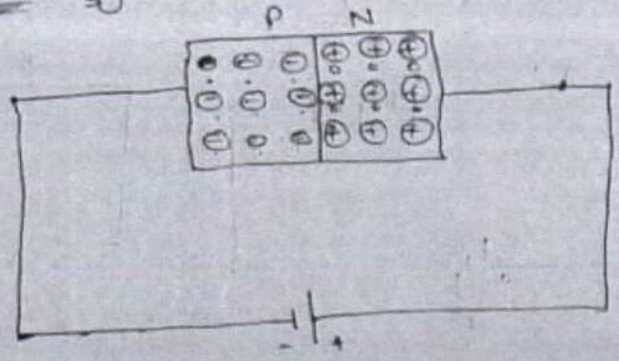




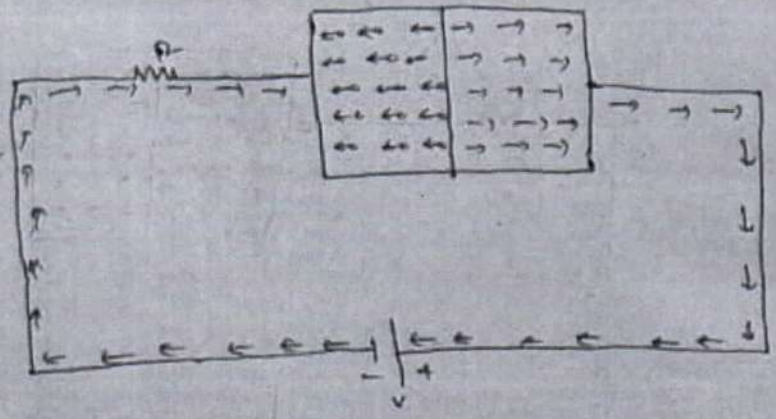
Reverse Bias of P-N Junction Diode:-



Deflection by:-



Operation on reverse Bias:-



2) The diode has two capacitance based on the electrical circuits are more sensitive at high efficiency. We have transition capacitance and Diffusion capacitance.

They are two types. They are.

i) transition capacitance.

ii) Diffusion capacitance.

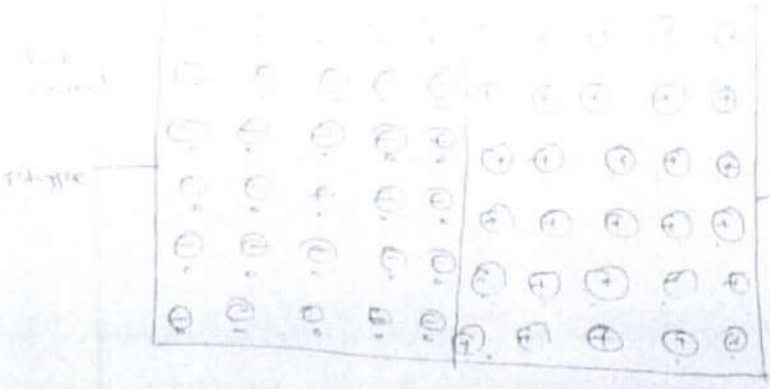
i) transition capacitance:-

When the diode is arranged in a forward bias the majority of the charge carriers of diffused. When the voltage is applied. The positive charge carrier like holes current are moved to p-N junction and electrons are moved to n-junction. The immobile charge carriers are in both junctions

ii) Diffusion capacitance:-

When the diode is arranged in a reverse bias the majority of charges carriers are moved through the reaction

$$D_o = \frac{V_i}{nt1}$$



B.Tech / M.Tech / MBA / MCA / B.Tech (R) LC1 2020 (A) 84317

Year II Semester I Sec D Test No 1

Sub Electronic Devices & Circuits Date 19/11/21

Name M.Anudya.

HALL TICKET NO

1	9	H	7	1	A	0	H	K	7

MARKS Tens: 1 Ones: 0 Marks in words: ONE ZERO

Signature of the Principal Signature of the Examiner - I Signature of the Examiner - II

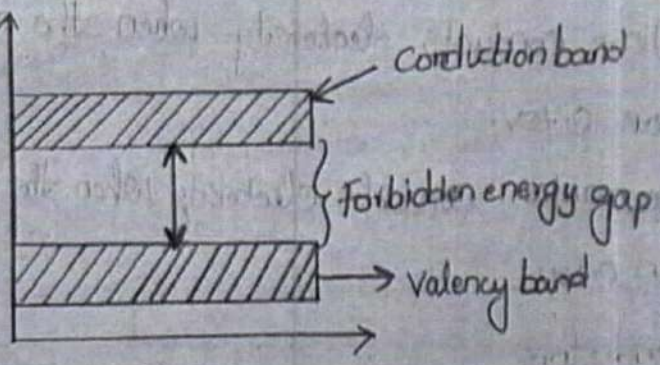
Answers

1. Energy band diagram contains (10)

1) conduction Band
2) Valence Band
3) Forbidden Energy gap.

Based on the forbidden Energy gap elements are classified as

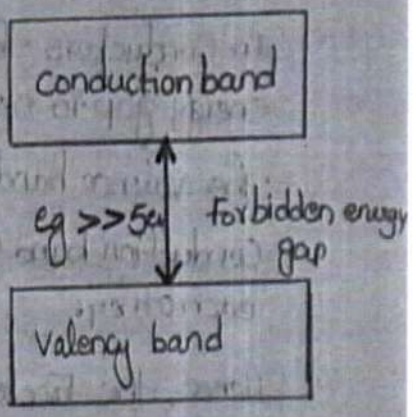
1) Insulators 2) semiconductors 3) conductors.



Insulators:-

In Insulators the Forbidden energy gap between Valency band and conduction band is greater than 5eV.

Hence the Free electrons cannot move from Valency band to conduction band.

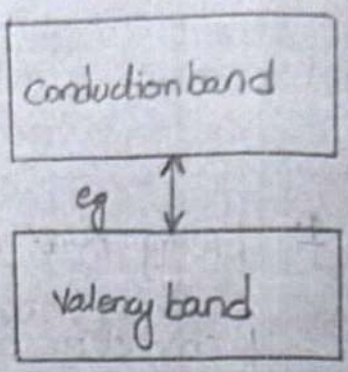


Ex: plastic, wood

Semiconductors

Semiconductors are the materials which posses both insulator and conduction based up on Application.

In semiconductors the forbidden energy gap between conduction band and valency band is very small.



So, Free electrons from valence band move from valence band to conduction band.

These valence band completely filled with free electrons.

Due to this they are called as semiconductors.

Ex:- silicon, Germanium.

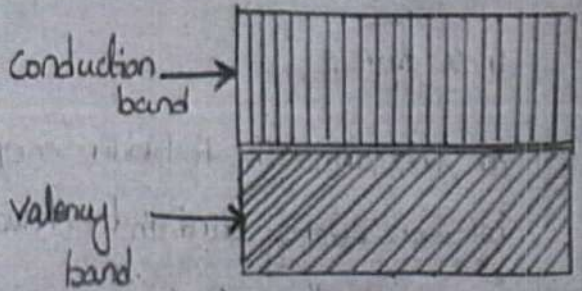
Silicon conducts electricity when the applied voltage is more than 0.7ev.

Germanium conducts electricity when the applied voltage is more than 0.3ev

Conductors

In Conductors the Forbidden energy gap is negligeble.

The valence band and Conduction band combine each other.



Hence, the Free electrons can easily move from Valence band

Hence, Due to this Free electoons they posses. Conductivity. the valence band completely filled with free electoons.

Conductors are the good metals for the better conductivity.

Ex:- Copper, Silver.

2. In forward bias, the depletion region is small. The size of the depletion region decreases due to the accumulation of holes and electoons.

In P-side the majority charge carriers are holes.

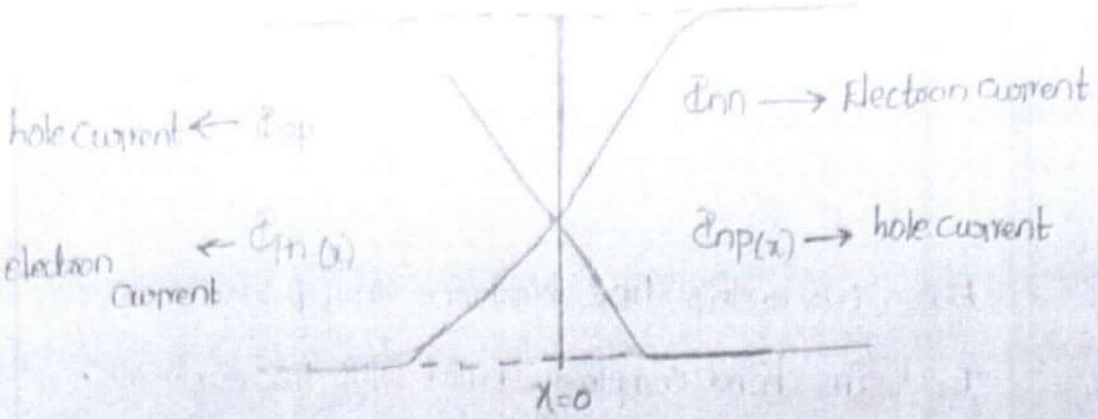
The minority charge carries are Electoons.

In Reverse bias, the size of the depletion region region increases due to cathode is connected to positive terminal of the battery and anode is connected to negative terminal of the battery. Electoons are attracted to positive terminal, holes are attracted to negative terminal.

In N-side the majority charge carriers are electoons.

The minority charge carriers are holes.

In P-side holes are diffuses into N-side so, the current caused in P-side is due to Electoons.



The in p-side electrons cause current, it is Diffusion current it Exponentially decreases with increase in temperature

In p-side holes are diffuse into N-side.

In N-side Electrons are diffused into p-side.

In N-side, the current is caused due to the holes. It is the Diffusion current, so it Exponentialy decreases with increase in temperature of voltage

I_{pp} – hole current in p-side

$I_{pn}(x)$ – Electron current in p-side

I_{nn} – Electron current in N-side

$I_{np}(x)$ – hole current in N-side.

P-side current

$$I = I_{pp} + I_{pn}(x)$$

$$I_{pp} = I - I_{pn}(x)$$

N-side current

$$I = I_{nn} + I_{np}(x)$$

$$I_{nn} = I - I_{np}(x)$$

NARASARAOPETA ENGINEERING COLLEGE, NARASARAOPET.

NEC

ASSIGNMENT TEST ANSWER BOOK

2020 (A) 8133I

B.Tech / M.Tech / MBA / MCA / D.Tech (Br.) ECE

Year II Semester II Grp D Test No 1

Sub Electronic Devices & Circuits Date 19-01-2021

Name A Vamsi Krishna

HALL TICKET NO

1	8	4	7	1	A	0	4	6	2

Tens Ones

MARKS 17 Marks in words Seventeen

Signature of the Principal Signature of the Examiner - I Signature of the Examiner - II

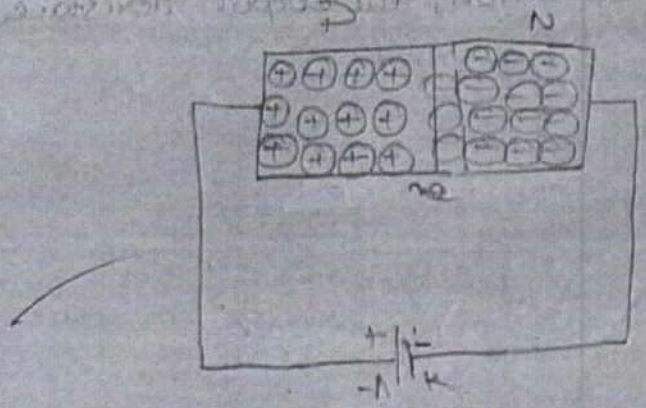
1. Diode is an Electric device. It joined p type material and n-type material is called pN junction diode. (4 A's = 0)

→ It allows only one direction of current

Operation P-N Junction in forward bias Condition (n-type Semi.)

When P-N Junction is connected in forward bias ~~the~~ negative voltage is applied to negative terminal and positive voltage applied to p-type Semiconductor. ~~and applied~~ If the External voltage becomes potential barriers. (Approximate Value Silicon 0.7) and when start current flowing.

→ When the Electrons are repulsion from n-type side therefore the Electrons towards the Junction as well as for holes are repulsion of p-type side therefore holes forwards the Junction.



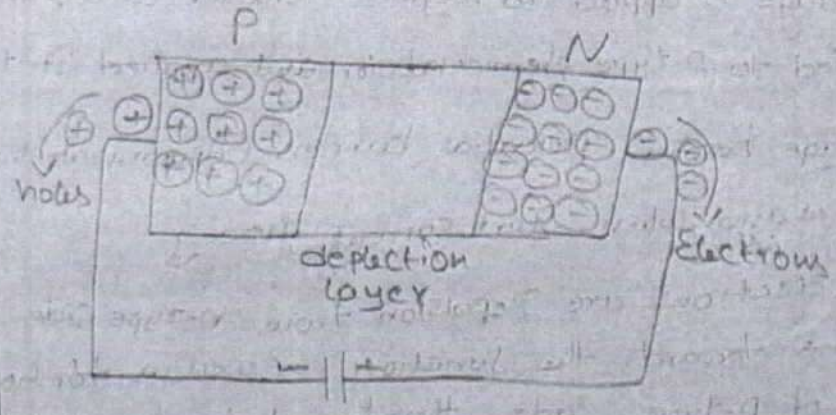
→ The above figure shows the diode connected in forward bias so it having very small depletion

In forward bias condition, the input resistance is very low

Preparation of P-N Junction diode in reverse bias condition

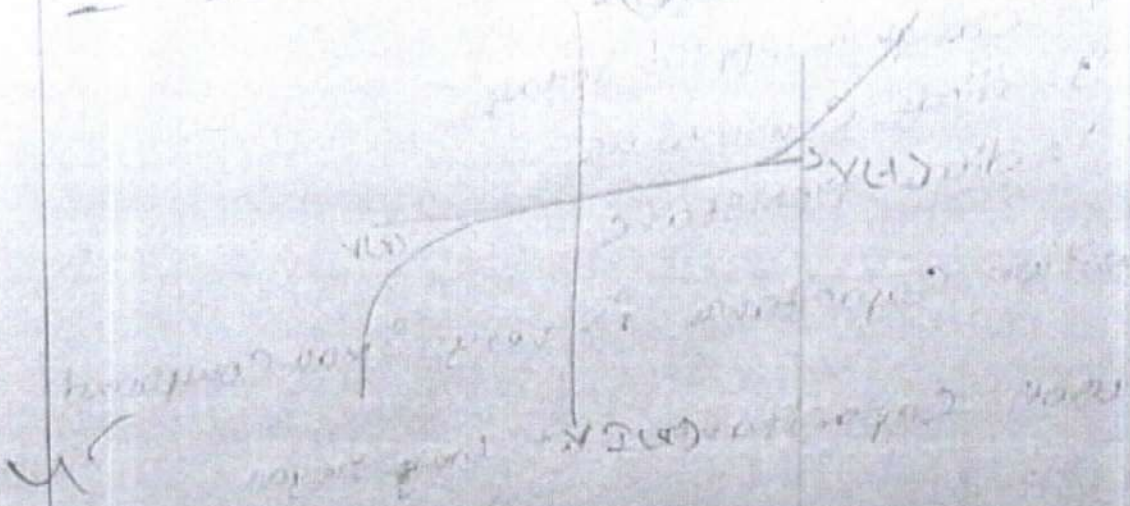
→ When P-N Junction is connected in reverse bias. that means when negative voltage is applied to p-type ~~and~~ Posi Semiconductor and positive voltage is applied to n-type Semiconductor

→ when the Electrons are attracted to positive voltage and holes are attracted to negative voltage! because increase the depletion layers.



→ In the above figure shows reverse bias condition In reverse bias condition, the output resistance is high.

V-I characteristics of P-N Junction



2. Generally Electronic devices are sensitive at high frequencies. The PN Semiconductor. Capacitance two types the transition capacitance or depletion capacitance and diffusion capacitance or storage capacitance. The capacitance can be formed two conditions such as forward bias condition and reverse bias condition.

Transitions Capacitation :- The capacitance appears the n-type layer at p-region and p-type layer at n-regine

diffusion capacitor

The capacitance originats due to the diode. In trasition capacitane in forward bias

CT = EA/d

CT = Transition capacito

E = premitivity

. W = width of depletion layer

Diffusion Capacitance in reverse bias

$$C_d = dQ/dV = \tau \times \frac{dI}{dQ} = \tau \times g = \tau / r$$

dQ = Change in charge
V = change in Applied Voltage
g = diode Conductance
r = diode resistance

Transition Capacitance is very small compound

Diffusion Capacitance at long regal

MID EXAM QUESTION PAPERS WITH SCHEME OF EVALUATION

NARASARAOPETA ENGINEERING COLLEGE (AUTONOMOUS)
NARASARAOPET

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II B.TECH I-SEMESTER MID-I Examinations, January -2021

SUBJECT: ELECTRONIC DEVICES AND CIRCUITS	DATE: 27-01-2021
DURATION: 90 MIN	MAX MARKS: 25M

Q. No		Questions	Course Outcome (CO)	Knowledge Levels as Per Bloom's Taxonomy	Max Marks
1	a	Utilize the energy band diagrams to classify semiconductors insulators and metals.	CO1	Applying (K3)	05
	b	Identify and explain the current components in a PN junction diode.	CO1	Applying (K3)	05
2	a	Utilize the energy band diagrams to explain the working and V-I characteristics of Tunnel diode.	CO2	Applying (K3)	05
	b	Make use of the circuit and necessary wave forms to explain the operation of half wave Rectifier.	CO2	Applying (K3)	05
3		Make use of the circuit and necessary input and output characteristics to explain Common base Configuration.	CO3	Applying (K3)	05

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II B.TECH I-SEMESTER MID-I Examinations, January -2021

SUBJECT: ELECTRONIC DEVICES AND CIRCUITS	DATE: 27-01-2021
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SCHEME OF EVALUATION

Q. No		Questions	Course Outcome (CO)	Knowledge Levels as Per Bloom's Taxonomy	Max Marks
1	a	Utilize the energy band diagrams to classify semiconductors insulators and metals.	CO1	Applying (K3)	05
		Energy band diagram -2M Explanation -3M			
	b	Identify and explain the current components in a PN junction diode.	CO1	Applying (K3)	05
		Current components diagram -2M Explanation -3M			
2	a	Utilize the energy band diagrams to explain the working and V-I characteristics of Tunnel diode.	CO2	Applying (K3)	05
		Energy band diagram -2M Explanation of working -3M			
	b	Make use of the circuit and necessary wave forms to explain the operation of half wave Rectifier.	CO2	Applying (K3)	05
		Circuit diagram -2M Wave forms -1M Explanation -2M			
3		Make use of the circuit and necessary input and output characteristics to explain Common base Configuration.	CO3	Applying (K3)	05
		Circuit diagram -2M Graph -1M Explanation of CB -2M			

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NARASARAOPET

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II B.TECH I-SEMESTER MID-II Examinations, MARCH -2021

SUBJECT: ELECTRONIC DEVICES AND CIRCUITS	DATE: 02-03-2021
DURATION: 90 MIN	MAX MARKS: 25M

Q. No		Questions	Course Outcome (CO)	Knowledge Levels as Per Bloom's Taxonomy	Max Marks
1	a	Compare different Transistor configurations with different parameters.	CO3	Analyzing (K4)	05
	b	Make use of circuit diagram to explain the Fixed bias circuit.	CO4	Applying (K3)	05
2	a	Compare the JFET and MOSFET with different parameters.	CO4	Analyzing (K4)	05
	b	Make use of circuit diagram to explain the construction and operation of UJT.	CO5	Applying (K3)	05
3		Identify the different types of MOSFETs and briefly explain the construction and operation of Enhancement mode MOSFET.	CO5	Applying (K3)	05

NARASARAOPETA ENGINEERING COLLEGE (AUTONOMOUS)
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II B.TECH I-SEMESTER MID-II Examinations, MARCH -2021

SUBJECT: ELECTRONIC DEVICES AND CIRCUITS	DATE: 02-03-2021
DURATION: 90 MIN	MAX MARKS: 25M

SCHEME OF EVALUATION

Q. No		Questions	Course Outcome (CO)	Knowledge Levels as Per Bloom's Taxonomy	Max Marks
1	a	Compare different Transistor configurations with different parameters.	CO3	Analyzing (K4)	05
		Any five different parameters -5M			
	b	Make use of circuit diagram to explain the Fixed bias circuit.	CO4	Applying (K3)	05
		circuit diagram -2M Explaination of the Fixed bias circuit -3M			
2	a	Compare the JFET and MOSFET with different parameters.	CO4	Analyzing (K4)	05
		Any five comparisons -5M			
	b	Make use of circuit diagram to explain the construction and operation of UJT.	CO5	Applying (K3)	05
		Circuit diagram -1M Explanation of the construction -2M Explanation of the operation of UJT -2M			
3		Identify the different types of MOSFETs and briefly explain the construction and operation of Enhancement mode MOSFET.	CO5	Applying (K3)	05
		Different types of MOSFETs -1M Explanation of the construction -2M Operation of Enhancement mode MOSFET. -2M			

NARASARAOPETA ENGINEERING COLLEGE:NARASARAOPET

DEPARTMENT OF ECE SET-III

QUIZ-II

II B.TECH I SEM

SUBJECT NAME : EDC

TIME : 20 MINUTES

MAX MARKS : 20x1/2=10M

DATE OF EXAM :

STUDENT NAME : P. Bhanu Appi

REGISTERED NO : 19491A04L4

BRANCH&SECTION : ECE-D

INVIGILATOR SIGNATURE :

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1. Ideally, for linear operation, a transistor should be biased so that the Q-point is [c]
a) near saturation b) near cutoff. c) where Ic is maximum.d) halfway between cutoff and saturation.

2.BJT stands for _____ [d]
a) Bi-Junction Transfer b) Blue Junction Transistor
c) Bipolar Junction Transistor d) Base Junction Transistor

3. a transistor _____ [D]
a) IC = IE + IB b) IB = IC + IE c) IE = IC – IB d) IE = IC + IB

4.The input/output relationship of the common-collector and common-base amplifiers is

a)270 degrees b) 180 degrees c) 90 degrees d) 0 degrees [d]

5. In a transistor highly doped part is
a) Emitter b) Base c) Collector d)None of the above [d]

6. For a transistor to operate in an active region what is the essential possible condition of biasing? [a]

a) Collector-base and emitter-base junctions are reverse biased.

b)Collector-base junction is reverse biased and the emitter-base is forward biased

c) Collector-base and emitter-base junctions are forward biased

d)Collector-base junction is forward biased and emitter-base is reverse biased

7. Which transistor bias circuit arrangement provides good stability using negative feedback from collector to base?
a) base bias b) collector-feedback bias c) voltage-divider bias d) emitter bias [a]

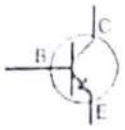
8. The most stable biasing technique used is the
a) voltage-divider bias. b) base bias. c) emitter bias. d) collector bias. [a]

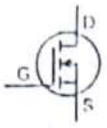
9. A diac is simply .....

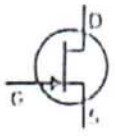
a) A single junction device b) A three junction device [a]

10. The point of intersection of d.c. and a.c. load lines represents ..... [a]
a) Operating point b) Current gain c) Voltage gain d) None of the above

11. Which symbol is n-channel JFET [c]

a) 

b) 

c) 

d) 

12. A JFET is also called _____ transistor [d]

a) unipolar b) bipolar c) unijunction d) none of the above

13. FETs are preferred to BJTs at high frequencies because they are [c]

a) Less noisy b) Capable of handling highest frequencies c) Easy to fabricate
d) All of the above

14. The UJT may be used as ..... [c]

a) An amplifier b) A sawtooth generator c) A rectifier d) None of the above

15. A Triac has three terminals viz ..... [c]

a) Drain, source, gate b)Two main terminal and a gate terminal c)Cathode, anode, gate d) None of the above

16. A FET is a.....controlled device whereas a bipolar transistor is a.....controlled device. [b]
a) Current, voltage b) Drain, gate c) Gate, drain d) Voltage, current

17. In P-channel FET the current is due to [b]
a) Electrons b) Holes c) Both holes and electrons d) Either holes or electrons

18.The drain of FET is analogous to..... of BJT [b]
a)Emitter b)Base c) Collector d) Substrate

19. An a UJT, the p-type emitter is ..... Doped [b]

a) Lightly b) Heavily c) Moderately d) None of the above

20. A triac has ..... semiconductor layers [b]

a) Two b) Three c) Four d) Five

NARASARAOPETA ENGINEERING COLLEGE::NARASARAOPET

DEPARTMENT OF ECE SET-IV

QUIZ-II

II B.TECH I SEM

SUBJECT NAME	: EDC	STUDENT NAME	: P. Sreeja
TIME	: 20 MINUTES	REGISTERED NO	: 19U71A04U3
MAX MARKS	: 20x1/2=10M	BRANCH&SECTION	: ECE-D
DATE OF EXAM	: 01/03/2021	INVIGILATOR SIGNATURE	:

---

1. For a transistor to operate in an active region what is the essential possible condition of biasing? [c]

a) Collector-base and emitter-base junctions are reverse biased.

b)Collector-base junction is reverse biased and the emitter-base is forward biased

c) Collector-base and emitter-base junctions are forward biased

d)Collector-base junction is forward biased and emitter-base is reverse biased

2.BJT stands for _____ [c]

a) Bi-Junction Transfer b) Blue Junction Transistor

c) Bipolar Junction Transistor d) Base Junction Transistor

3. a transistor _____ [b]

a) IC = IE + IB b) IB = IC + IE c) IE = IC – IB d) IE = IC + IB

4. The most stable biasing technique used is the [0]

a) voltage-divider bias. b) base bias. c) emitter bias. d) collector bias.

5. The UJT may be used as..... [c]

a) An amplifier b) A sawtooth generator c) A rectifier d) None of the above

6. Ideally, for linear operation, a transistor should be biased so that the Q-point is [b]

a) near saturation b) near cutoff. c) where I_C is maximum.d) halfway between cutoff and saturation.

7. In a transistor highly doped part is [a]

a) Emitter b) Base c) Collector d)None of the above

8. The point of intersection of d.c. and a.c. load lines represents ..... [a]

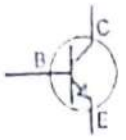
a) Operating point b) Current gain c) Voltage gaind) None of the above

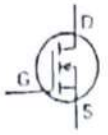
9.The input/output relationship of the common-collector and common-base amplifiers is [c]

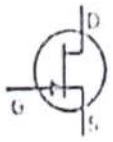
a)270 degrees b) 180 degrees c) 90 degrees d) 0 degrees

10. Which transistor bias circuit arrangement provides good stability using negative feedback from collector to base?
a) base bias b) collector-feedback bias c) voltage-divider bias d) emitter bias

11. Which symbol is n-channel JFET

a) 

b) 

c) 

d) 

12. A JFET is also called _____ transistor

a) unipolar b) bipolar c) unijunction d) none of the above

13. FETs are preferred to BJTs at high frequencies because they are

a) Less noisy b) Capable of handling highest frequencies c) Easy to fabricate
d) All of the above

14. A diac is simply .....

a) A single junction device b) A three junction device c) A triac without gate terminal

d) None of the above

15. A Triac has three terminals viz .....

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16. A FET is a.....controlled device whereas a bipolar transistor is a.....controlled device.
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NARASARAOPETA ENGINEERING COLLEGE::NARASARAOPET

DEPARTMENT OF ECE SET-III

QUIZ-II

II B.TECH I SEM

SUBJECT NAME : EDC

TIME : 20 MINUTES

MAX MARKS : 20x1/2=10M

DATE OF EXAM :

STUDENT NAME : B. Leela Krishna Kumar

REGISTERED NO : 20[illegible]A0402

BRANCH&SECTION : ECE - D

INVIGILATOR SIGNATURE :

---

1. Ideally, for linear operation, a transistor should be biased so that the Q-point is [d]
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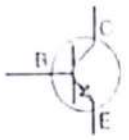
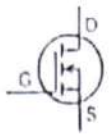
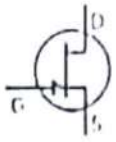
a) 

b) 

c) 

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18.The drain of FET is analogous to..... of BJT [c]
a)Emitter b)Base c) Collector d) Substrate

19. An a UJT, the p-type emitter is ..... Doped [b]

a) Lightly b) Heavily c) Moderately d) None of the above

20. A triac has ..... semiconductor layers [d]

a) Two b) Three c) Four d) Five

NEC

MAIN ANSWER BOOK

2021 (A) 00053

HALL TICKET NO

Name: G. Satyanarayana

Date: 2/03/21

MARKS: 2 | 1 | Marks in words: One | Fifty

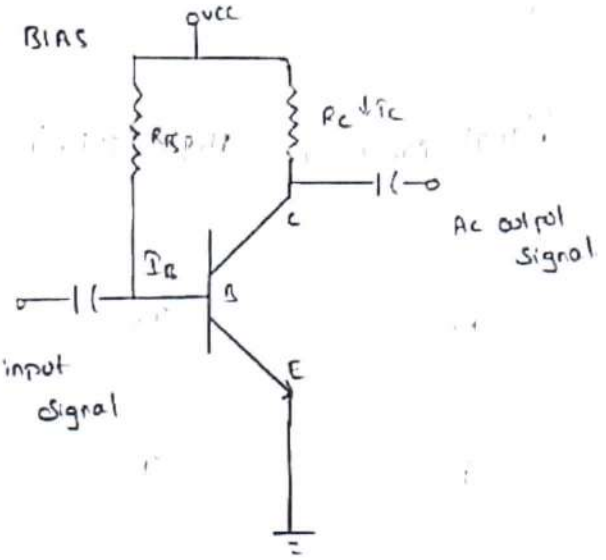
Signature of the Principal | Signature of the Examiner - I | Signature of the Examiner - II

(1) a) Transistor configuration with different parameters

CHARACTERISTICS	COMMON BASE CONFIGURATION	COMMON EMMITTER CONFIGURATION	COMMON COLLECTOR CONFIGURATION
Input Resistance	very low (100 Ω)	low (750 Ω)	High (10MΩ)
Output Resistance	High (400kΩ)	High (50kΩ)	low (500Ω)
Input current	I_B	I_B	I_C
Output current	I_C	I_C	I_B
Input voltage	Emitter & Base	Base & Emitter	Base & Collector
Input output voltage	Collector & Base	Collector & Emitter	Emitter & Collector

Current Amplification (αdc)	$\alpha_{dc} = \frac{I_c}{I_e}$	$\beta_{dc} = \frac{I_c}{I_B}$	$\gamma = \frac{I_c}{I_B}$
Current gain	less than unity	high (> 50 to 500)	high (> 10,000 to 500)
Voltage gain	Medium (150)	Medium (500)	Low (< 1)
Applications	As input stage Multistage Amplification	RF Radio Signal Amplification	Impedance Matching

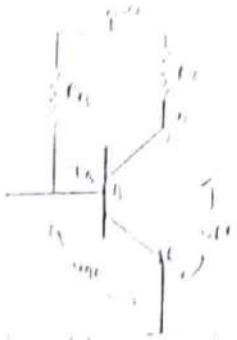
b) FIXED BIAS



For DC Analysis The capacitor becomes open circuit. The Resistance of capacitor for DC is

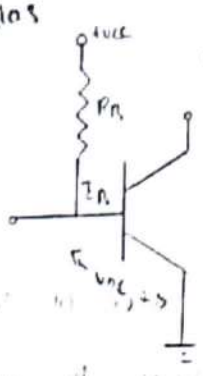
$$X_c = \frac{1}{2\pi fc} = \frac{1}{2\pi(0)c} = \infty$$

Equivalent Circuit diagram



Analysis

Base Bias



Apply kirchoff's voltage law to Base Bias

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CE} = I_B R_B + V_{CC}$$

$$I_B R_B \cong V_{CC} - V_{CE}$$

$$\boxed{I_B = \frac{V_{CC} - V_{CE}}{R_B}}$$

Here Collector Bias is Empty Because it is Base Bias

Collector Bias

Apply kirchoff's voltage law to collector bias

$$V_{cc} - I_c R_c - V_{ce} = 0$$

$$V_{cc} = I_c R_c + V_{ce}$$

$$I_c R_c = V_{cc} - V_{ce}$$

$$\boxed{I_c = \frac{V_{cc} - V_{ce}}{R_c}}$$

Base current controlled by the value of I_c. Related to I_B by constant β I_c will increase to any level will not affect the Resistance R_c. I_c is change will at V_{cc}

$$V_{ce} = V_B - V_E$$

$$V_{cc} = V_B - V_E$$

$$V_E = 0$$

V_E = Emitter voltage

V_c = collector voltage

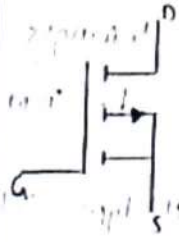
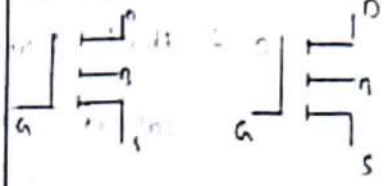
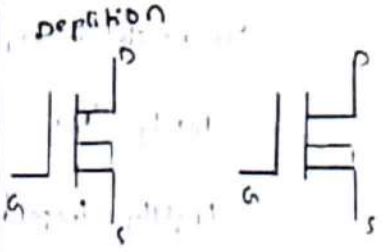
V_B = Base voltage

$$V_{ce} = V_E$$

$$V_{BE} = V_B$$

(2) Compare the JFET & MOSFET with different parameters

a)

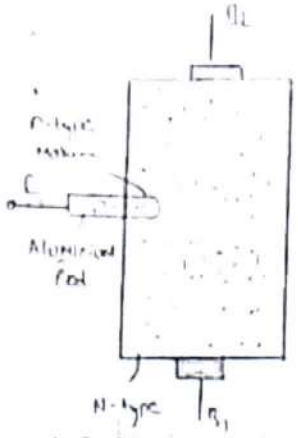
parameters	JFET	MOSFET
types	a) n channel b) p channel	a) n channel depletion b) p channel depletion c) n channel enhancement d) p channel enhancement
Operation mode	operation in depletion Region	operation in depletion and enhancement Region
Gate	Gate is not insulated in depletion	Gate is insulated in depletion by layer of SiO_2
Channel	Channels are from depletion Region	Channels are from depletion Region . Not not from Enhancement Region
Symbols	depletion  a) N-channel  b) P-channel	enhancement  a) N-channel b) P-channel depletion  a) N-channel b) P-channel

(5)

a) UJT:

It does not belongs to thyristor family but it used to turn on SCR

Construction :-



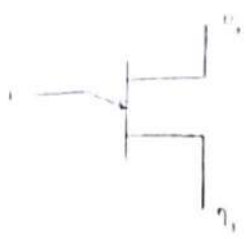
There are three terminals. lightly dopped in N-type Slab Silicon Material Both Base are attached to the end ~~la~~ of the N-type Silicon Material Those are Base (B_1) and Base (B_2)

Three terminals Both are Base 1 & Base 2 and third terminal is P type Material hevily dopped is called Emitter.

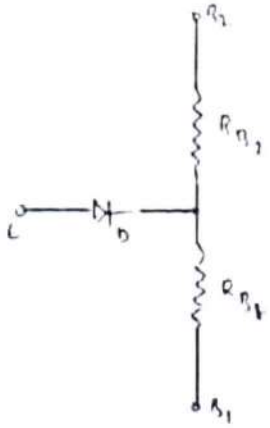
Aluminium Rod is used in UJT. (Uni-junction Transistor) UJT does not belongs to thyristors family but it is used to TURN ON SCR

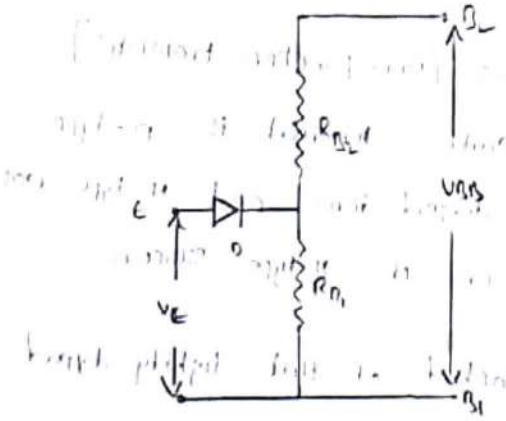
Lighly dopped Slab are N-type silicon and hevily dopped e' are P-type Material & called Emitter

6. Symbol of UJT



Equivalent circuit of UJT





$R_{BB} = R_{B_1} + R_{B_2}$

$I_E = 0$

$R_{BB} = R_{B_1} + R_{B_2}$

$I_E = 0$

Voltage across R_{BB} at $I_E = 0$.

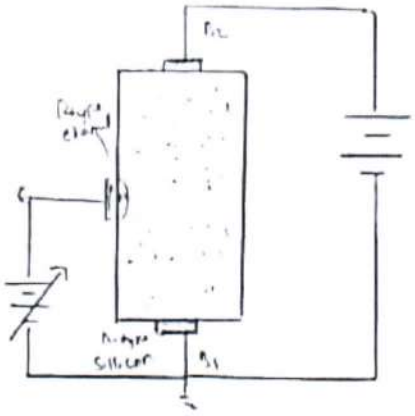
$V_{BB} = \frac{R_{B_1}}{}$

$$V_{BB} = \frac{R_{BB} \cdot V_{CC}}{R_{B1} + R_{B2}} \quad [R_{BB} = R_{B1} + R_{B2}]$$

$$= \frac{V_{BB} \cdot R_{B1}}{R_{BB}}$$

$$= \frac{R_{B1}}{R_{BB}}$$

Principle of operations :



The operations of UJT [uni-junction transistor] variable & constant emitter terminal is p-type channel has hevily dopped ions and N-type are attached at the end of N-type silicon

B_1 & B_2 are attached at that lightly dopped ions are placed at there.

prinples of the operation variable & constant places

The three terminals are Emitter, Base$_1$ & Base$_2$

UJT

B.Tech / M.Tech / MBA / MCA / B-Tech (Regular) ECE | 2021 (A) | 10984

Year II Semester I Set No. 4

Sub EDC Date

Name T. Bindu Madhuri

HALL TICKET NO: 1 4 4 J 1 A 0 4 1 1 0

MARKS: 07 (Tens: 0, Ones: 7) Marks in words: Zero Seven

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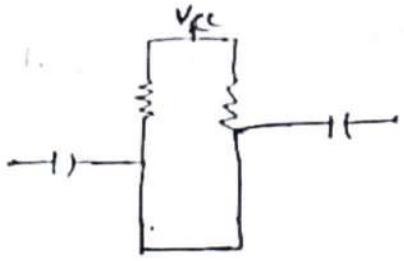
1 b

Transistor

fixed bias circuit



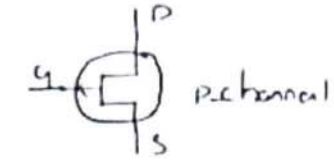
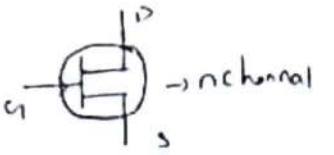
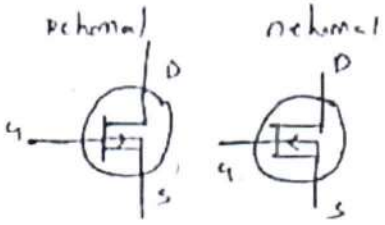
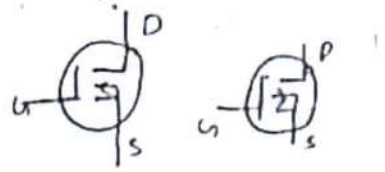
In fixed bias

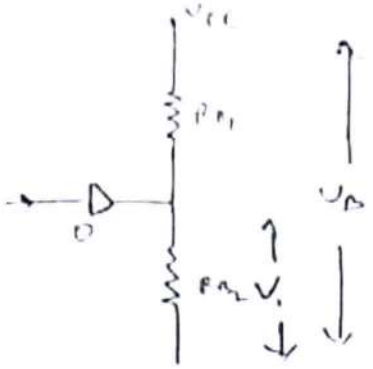
(1) $V_{CC} - (I_B R_B) - V_{BE}$

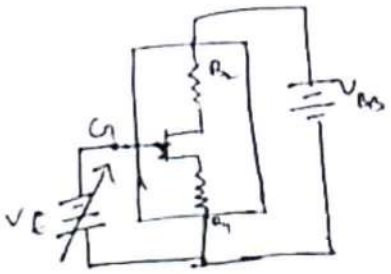
$V_{CC} = I_B R_B - V_{BE}$

$I_B R_B = V_{CC} + V_{BE}$

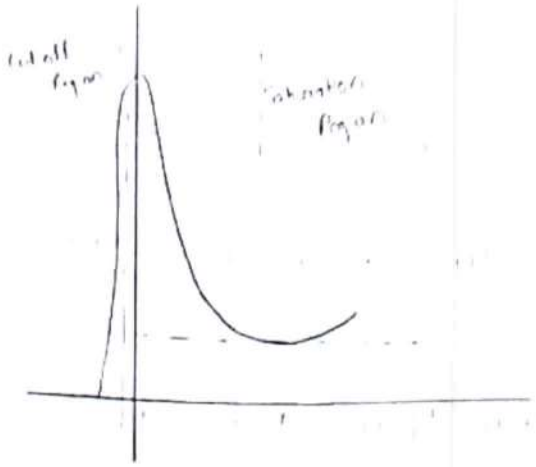
$I_B R_B = \frac{V_{CC} + V_{BE}}{R_B}$

Parameter	JFET	MOSFET
Type	n-channel p-channel	n-channel depletion p-channel depletion Enhancement p-channel enhancement n-channel enhancement
operation mode	it operates Depletion layer	it operate both depletion and Enhancement layer.
Input Impedance	input impedance (>10 MΩ)	(10,000 MΩ)
Gate		
channel segment	 	 



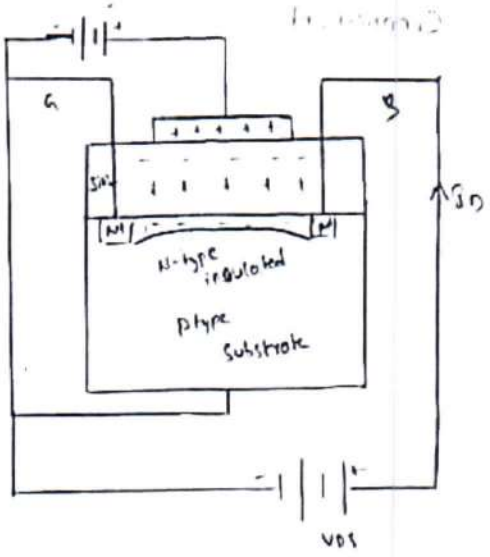


-2- UJT is an unijunction diode & consists of one gate and and B_1 and B_2 are two parts connect the the gate Then the circuit can be written are as V_{B_1} and V_{B_2} and The Resistance are R_{B_1} and R_2 are the in UJT.

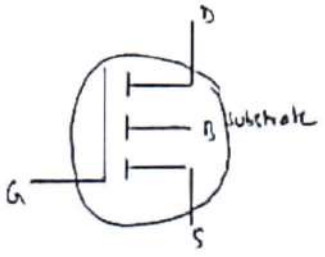


(3) MOSFET

ENHANCEMENT MODE MOSFET



Symbol of MOSFET



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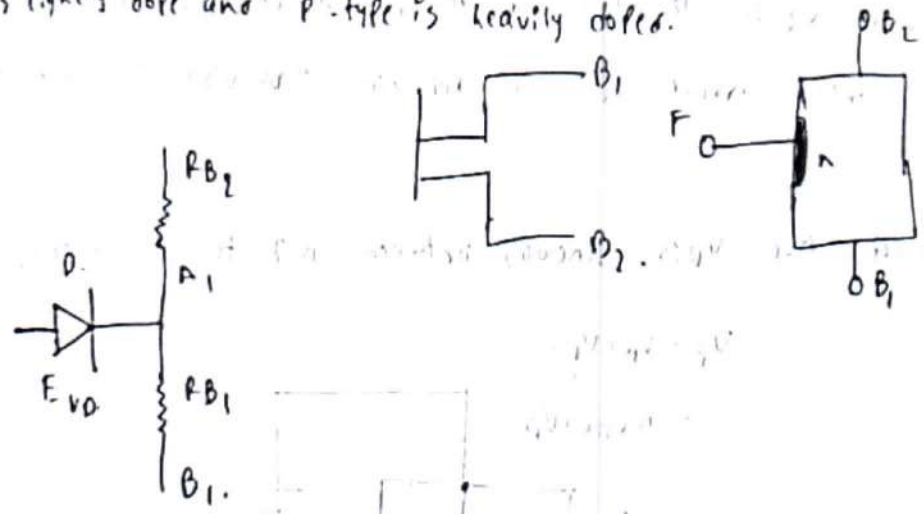
5)

b) UJT :- it is three terminal device it consists of a slate lightly dope n type silicon material the two base contact are attached to both ends of n-type surface they are B_1 and B_2 n-type material is used to form a p-n junction this method third terminal is called emitter the n type is lightly dope and p-type is heavily doped.



Instruction stand of ratio(η):-

Then $R_{BB} = R_{B_1} + R_{B_2}$

voltage across R_{B_1} is

$$R_{D_1} = \frac{R_{B_1} + V_{BB}}{R_{B_1} + R_{B_2}} \quad V_{BB}$$

if put the emitter diode reverse biased for all the emitter voltage less than V_{BB}.

$$\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}$$

$$\eta = \frac{R_{B_1}}{R_{BB}}$$

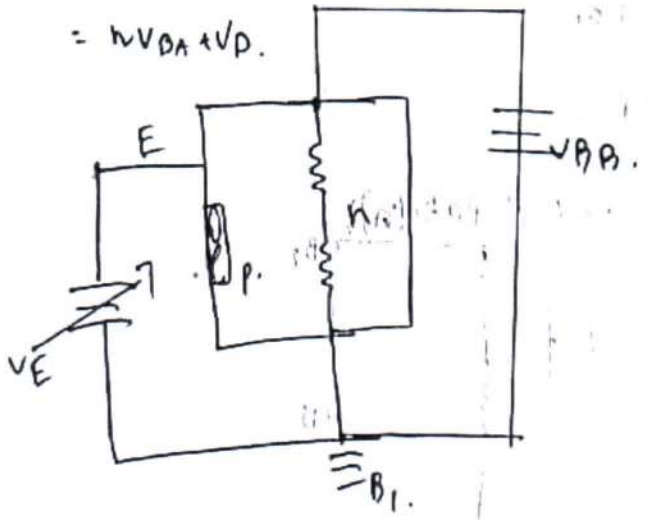
when operating an UJT the supply V_{BB} is applied between B_2 and B_1 variable emitter voltage V_E is applied across the emitter terminals the potential A is decided by η and is equal to ηV_{BB} even if $V_E < V_A$.

As long as V_E is less than V_A the p-n junction is reverse biased when emitter current I_E will not flow thus UJT is said to be off.

The diode drop V_D is generally between 0.7 to 0.7V Hence.

$$V_P = V_A + V_D.$$

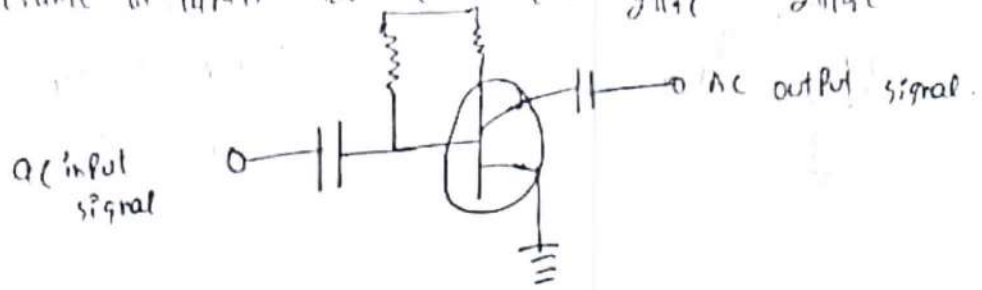
$$= \eta V_{BA} + V_D.$$

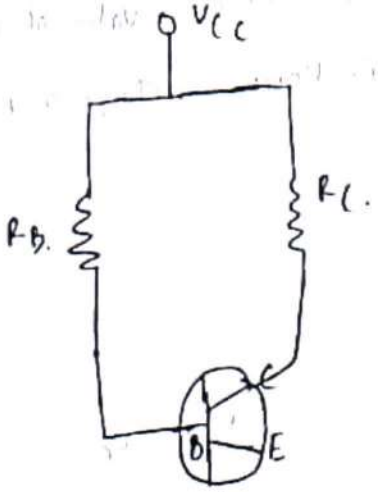


b) fixed circuit:

for dc analysis the capacitor can replace with an open circuit because

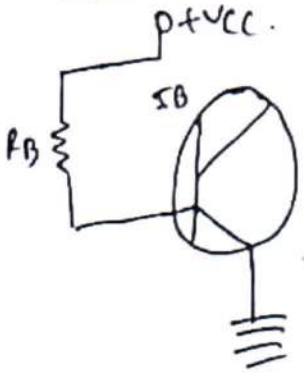
reactance of capacitor for dc is $X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi(0)C} = \infty$





circuit analysis:-

base circuit:-



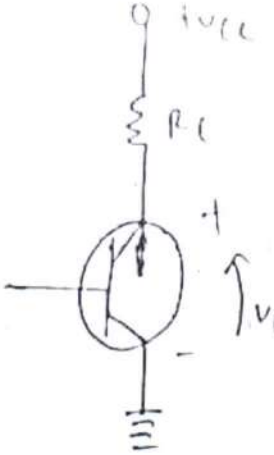
Applying KVL to base circuit

$V_{CC} - I_B R_B - V_{BE} = 0$

$V_{CC} = I_B R_B + V_{BE}$

$I_B R_B = V_{CC} - V_{BE}$

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$



Applying KVL to collector circuit

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = I_C R_C - V_{CC}$$

$$I_C R_C = V_{CC} - V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

The base current is controlled by the value of R_B and I_C is the I_B related by a constant B. However. Change in R_C will change the value of V_{CE}.

$$V_{CE} = V_C - V_E.$$

$$V_{BE} = V_B - V_E$$

Here $V_E = 0$.

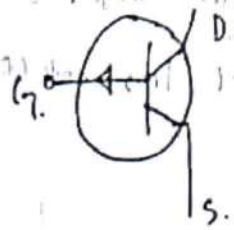
$$V_{CE} = V_C$$

$$V_{BE} = V_B.$$

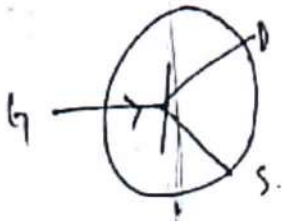
(9) Comparison of JF

parameter	JFET	MOSFET
Types	a) n-channel. b) p-channel.	a) n channel depletion. b) p-channel depletion. c) n-channel depletion. d) p-channel depletion.
operation mode	operated in depletion mode.	operated depletion and enhancement mode.
Input impedance.	High ($710 M\Omega$)	Very high ($7 \log \Omega$).
Gate	Gate is not insulated from channel.	Gate is insulated from a channel by a layer of SiO_2.
Channel.	Channel exits in permanently.	Channel exits permanently in depletion or type MOSFET but not in enhancement MOSFET depletion

Symbols.

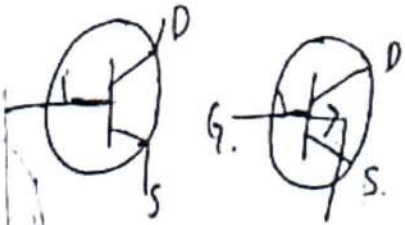


p-channel.

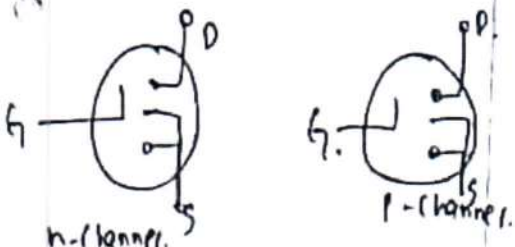


n-channel.

Depletion:

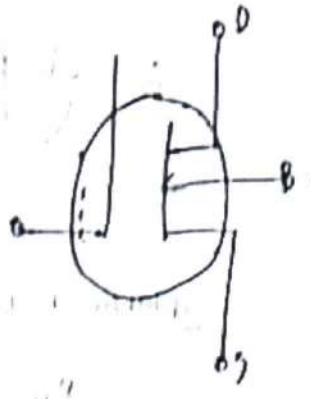


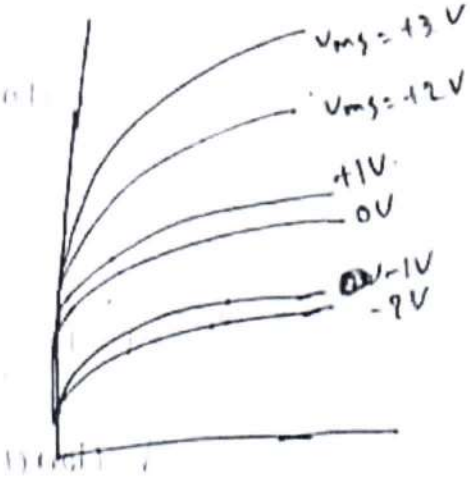
Enhancement channel:

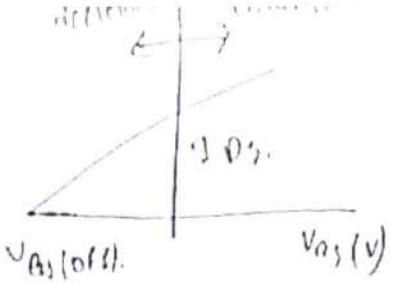


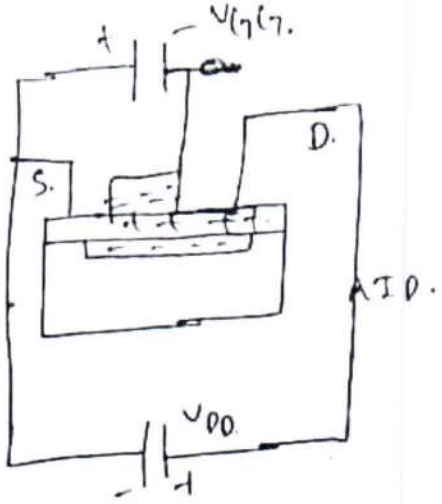
* mosfet differs from the JFET in that it has metal gate electrode which the gate of the mosfet is insulated from the channel by a silicon dioxide layer due to this the input resistance of mosfet is greater than JFET because of the insulated gate mosfet are also called IGFET, in drain through the induced channel this drain current is controlled by positive gate voltage with $V_{GS}=0$ and the drain plays no role in controlling the electrons flows through the n-channel from S to D. therefore the conventional current I_D flows through channel D to S. if the gate voltage is made negative positive charge consists of holes is induced in channel through side of the gate channel capacitor.

* the current in FET is due to majority carriers the induced positive charge makes the channel less conductive and I_D drops as V_{GS} is made negative






I_{DS}.
$V_{GS(off)}$.
V_{GS} (V)


V_{GG}.
D.
S.
AIO.
V_{DD}.

END EXAM QUESTION PAPER WITH KEY

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

II B.Tech I Semester Regular Examinations, March-2021

Sub Code: 19BEC3TH02 ELECTRONIC DEVICES AND CIRCUITS

Time: 3 hours (ECE) Max. Marks: 60

Note: Answer All FIVE Questions.

All Questions Carry Equal Marks (5 X 12 = 60M)

Q.No		Questions	Marks
		Unit-I	
1	a	i) Explain the semiconductors, insulators and metals classification using energy band	[6M]
		ii) Find the concentration of holes and electrons in a p-type germanium at 3000K, if the conductivity is 100Ω-cm. mobility of holes in germanium μp = 1800cm2 /Vsec	[6M]
		OR	
	b	i) Explain the Diffusion and Drift currents for a semiconductor	[6M]
		ii) Show that the Fermi energy level lies in the centre of forbidden energy band for an intrinsic semiconductor? Derive	[6M]
		Unit-II	
2	a	Explain the following diodes in detail (i) LED (ii) LCD (iii) Photodiode	[12M]
		OR	
	b	i) Explain the construction and working of Zener diode along with diagram	[4M]
		ii) With circuit and necessary waveforms explain the operation of bridge rectifier	[4M]
		iii) Compare and contrast Zener breakdown and Avalanche breakdown	[4M]
		Unit-III	
3	a	i) Explain input and output characteristics of common emitter configuration along with characteristics	[6M]
		ii) Explain the concept of Transistor Current Components in detail	[6M]
		OR	
	b	i) Explain the Relation among α, β, and γ in detail	[6M]
		ii) List out few comparisons of CB, CE and CC Configurations along with examples	[6M]
		Unit-IV	
4	a	i) What is thermal runaway? Derive relevant expressions to obtain thermal stability	[6M]
		ii) In a silicon transistor with a fixed bias, Vcc= 9 V, Rc= 3 kΩ, RB= 8kΩ, β = 50, V_{BE}= 0.7V. Find the operating point and stability factor	[6M]
		OR	
	b	i) What is Biasing? Explain the need of it. List out different types of biasing methods	[6M]
		ii) With the help of neat diagram explain the voltage divider biasing method for Transistor.	[6M]
		Unit-V	
5	a	i) Draw the construction diagram, operation characteristics and parameters of JFET	[6M]
		ii) Draw and explain the working operation of SCR along with characteristics	[6M]
		OR	
	b	i) Explain the construction and working of Enhancement MOSFET	[6M]
		ii)Write short notes on UJT-Negative Resistance Property in detail	[6M]

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NARASARAOPETA ENGINEERING COLLEGE(AUTONOMOUS)

II B.Tech I Semester Regular Examinations,March-2021

Subject Code:**19BEC3TH02**

Subject Name:**ELECTRONIC DEVICES AND CIRCUITS**

Answer All FIVE Questions & All Questions carry equal marks (5x12=60 Marks)

Q.No		Questions	Marks
		UNIT-I	
1	a(i)	Conductors are generally substances which have the property to pass different types of energy. In the following, the conductivity of electricity is the value of interest. **METALS** The conductivity of metals is based on the free electrons (so-called Fermi gas) due to the metal bonding. Already with low energy electrons become sufficiently detached from the atoms and a conductivity is achieved. The conductivity depends, inter alia, on the temperature. If the temperature rises, the metal atoms swing ever stronger, so that the electrons are constrained in their movements. Consequence, the resistance increases. The best conductors, gold and silver, are used relatively rare because of the high costs (gold e.g. for the contacting of the finished chips). The alternatives in the semiconductor technology for the wiring of the individual components of microchips are aluminum and copper. **INSULATORS** Insulators possess no free charge carriers and thus are non-conductive. **The atomic bond** The atomic bond is based on shared electron pairs of nonmetals. The elements which behave like nonmetals have the desire to catch electrons, thus there are no free electrons which might serve as charge carriers. **The ionic bond** In the solid state, ions are arranged in a grid network. By electrical forces, the particles are held together. There are no free charge carriers to enable a current flow. Thus substances composed of ions can be both conductor and insulator. **SEMICONDUCTORS** Semiconductors are solids whose conductivity lies between the conductivity of conductors and insulators. Due to exchange of electrons - to achieve the noble gas configuration - semiconductors arrange as lattice structure. Unlike metals, the conductivity increases with increasing temperature. Increasing temperatures leads to broken bonds and free electrons are generated. At the location at which the electron was placed, a so-called defect electron ("hole") remains. **The band model** The electronic band structure is an energy schema to describe the conductivity of conductors, insulators, and semiconductors. The schema consists of two energy bands (valence and conduction band) and the band gap. The valence electrons - which serve as charge carriers - are located in the valence band, in the ground state the conduction band is occupied with no electrons. Between the two energy bands there is the band gap, its width affects the conductivity of materials. The energy bands If we consider a single atom, there are according to the Bohr model of atoms	06M

sharply distinct energy levels, which may be occupied by electrons. If there are multiple atoms side by side they are interdependent, the discrete energy levels are fanned out. In a silicon crystal, there are approximately 1023 atoms per cubic centimeter, so that the individual energy levels are no longer distinguishable from each other and thus form broad energy ranges.

The band model of conductors

In conductors, the valence band is either not fully occupied with electrons, or the filled valence band overlaps with the empty conduction band. In general, both states occure at the same time, the electrons can therefore move inside the partially filled valence band or inside the two overlapping bands. In conductors there is no band gap between the valence band and conduction band.

The band model of insulators

In insulators the valence band is fully occupied with electrons due to the covalent bonds. The electrons can not move because they're "locked up" between the atoms. To achieve a conductivity, electrons from the valence band have to move into the conduction band. This prevents the band gap, which lies in-between the valence band and conduction band.

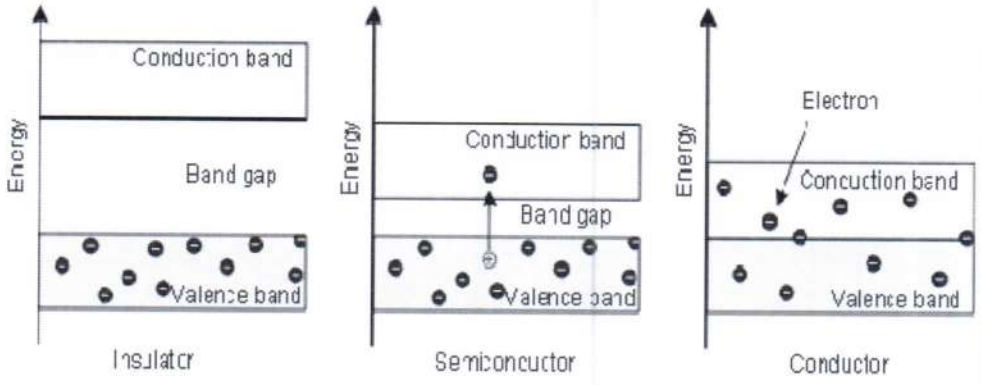
Only with considerable energy expenditure (if at all possible) the band gap can be overcome; thus leading to a negligible conductivity.

The band model of semiconductors

Even in semiconductors, there is a band gap, but compared to insulators it is so small that even at room temperature electrons from the valence band can be lifted into the conduction band. The electrons can move freely and act as charge carriers. In addition, each electron also leaves a hole in the valence band behind, which can be filled by other electrons in the valence band. Thus one gets wandering holes in the valence band, which can be viewed as positive charge carriers.

There are always pairs of electrons and holes, so that there are as many negative as positive charges, the semiconductor crystal as a whole is neutral. A pure undoped semiconductor is known as intrinsic semiconductor. Per cubic centimeter there are about 1010 free electrons and holes (at room temperature).

Since the electrons always assume the energetically lowest state, they fall back into the valence band and recombine with the holes if there is no energy supply. At a certain temperature an equilibrium is arranged between the electrons elevated to the conduction band and the electrons falling back. With increasing temperature the number of electrons that can leap the band gap is increased, and thus increasing the conductivity of semiconductors.



	a(ii)	Assume n_i=2.5x10^{19} cm^{-3} Concentration of holes=$\frac{\sigma}{q.\mu p}$=3.47x10^{21} cm^{-3} Concentration of electrons = $\frac{(ni)2}{p}$ = 0.72x10^{17} cm^{-3}	06M
		OR	
	b(i)	Drift and diffusion are responsible for generating current in semiconductors and the overall current density is the sum of the drift and diffusion currents. There are two types of current through a semiconducting material – one is drift	

current and the other is diffusion current. The mechanism of drift current is similar to the flow of charge in a conductor. In case of conductor when a voltage is applied across the material, the electrons are drawn to the positive end. Similar is the case in semiconductor. However, the movement of the charge carriers may be erratic path due to collisions with other atoms, ions and carriers. So, the net result is a drift of carriers to the positive end. 06M

In semiconducting material, when a heavy concentration of carrier is introduced to some region, the heavy concentrations of carriers distribute themselves evenly through the material by the process of diffusion. It should be remembered that there is no source of energy as required for drift current. When an electric field is applied across the crystal, every charge carrier experiences a force due to the electric field and hence it will be accelerated in the direction of force. This results in drifting of the charge carriers in the direction of force will cause a net flow of electric current through the crystal.

The magnitude of this current can be obtained by imagining an average drift velocity for every charge carrier in the direction of force. As the electrons and holes are of opposite charges, the force due to electric field on them will be opposite in direction. Hence the average drift velocity of the electrons will be in a direction opposite to the average drift velocity of the holes.

Diffusion Current: The movement of charge carriers from higher concentration to lower concentration generates diffusion current. This occurs when a semiconductor is doped non-uniformly then there is a non-uniform distribution of carriers or a concentration gradient.

Nature's way of attaining equilibrium in this case is through diffusion of particles (carriers) and this gives rise to a diffusion current.

Quite simply, the current moves in the same direction as the movement of holes and opposite to that of electrons.

Let Vh = average drift velocity of holes

Ve = average drift velocity of the electrons.

Vh α E => Vh= μh E and Ve α E => Ve= μe E , where μh ,μe are the hole and electron mobility and positive quantity.

Also we may say the mobility of the charge carriers are the average drift velocity per unit electric field applied.

Now the drift current density for hole and electrons are given by

J_{h1} = p e Vh and J_{e1} = - n e Ve ,

where n,p are the electron and hole densities. Negative sign indicates that the electrons having -ve charge move in direction opposite to the applied field.

Total drift current density Jd = Jh1 + Je1 = p e V_h – n e V_e

= p e μ_h E + n e μ_e E

= (p μ_h + n μ_e) e E

b(ii)

n_e = number of electrons in the semiconductor band.

n_v= number of holes in the valence band.

At any temperature, T>0K

$n_e = N_c.e^{-(Ec-EF)/kT}$ and

$n_v = N_v.e^{-(EF-Ec)/kT}$

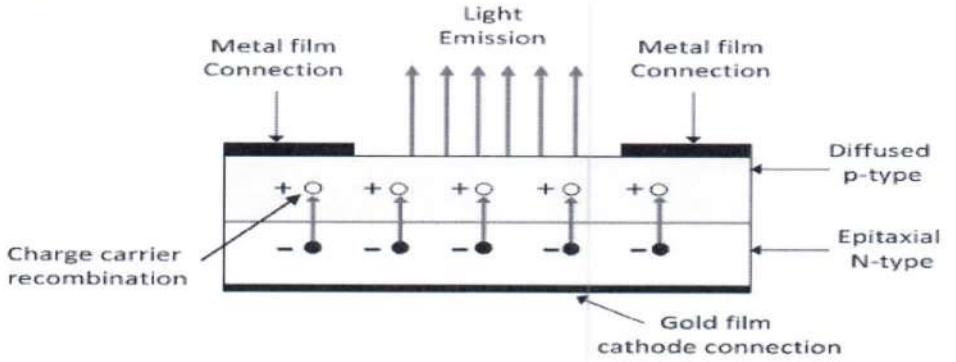
Where, N_c is the effective density of states in the conduction band. N_v is the effective density of states in the valence band.

For best approximation, $N_c = N_v$

For an intrinsic semiconductor, $n_e = n_v$ 06M

$N_c.e^{-(Ec-E_F)/kT} = N_v.e^{-(E_F-Ec)/kT}$

$\{e^{-(Ec-EF)/kT}\} / \{e^{-(EF-Ec)/kT}\} = Nv / Nc$

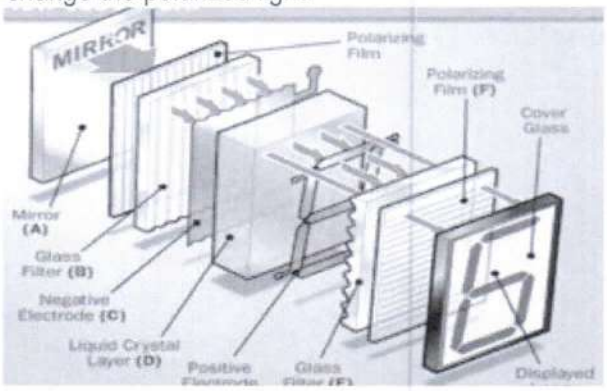
		$e^{-(E_C+E_V+2E_F)/kT}=1$ (Nc=Nv) Taking ln on both sides, $-(E_C+E_V-2E_F) / kT = 0$ $E_F=(E_C+E_V) / 2$ Thus, Fermi level in an intrinsic semiconductor lies at the centre of the forbidden gap.	
2	a	**LED:**LED is a particular diode which generates photons (light) when a stream of electrons passes through it. To build a diode we use a crystal (electric insulator) which is doped by atoms which have one more electron on their valence band (N doping) or missing one electron on their valence band (P doping). **Construction&Working** The recombination of the charge carrier occurs in the P-type material, and hence P-material is the surface of the LED. For the maximum emission of light, the anode is deposited at the edge of the P-type material. The cathode is made of gold film, and it is usually placed at the bottom of the N-region. This gold layer of cathode helps in reflecting the light to the surface.  The gallium arsenide phosphide is used for the manufacturing of LED which emits red or yellow light for emission. The LED are also available in green, yellow amber and red in colour. The LED is connected in the forward biased, which allows the current to flows in the forward direction. The flow of current is because of the movement of electrons in the opposite direction. The recombination shows that the electrons move from the conduction band to valence band and they emits electromagnetic energy in the form of photons. The energy of photons is equal to the gap between the valence and the conduction band. **Working of LED** The working of the LED depends on the quantum theory. The quantum theory states that when the energy of electrons decreases from the higher level to lower level, it emits energy in the form of photons. The energy of the photons is equal to the gap between the higher and lower level. The LED is connected in the forward biased, which allows the current to flows in the forward direction. The flow of current is because of the movement of electrons in the opposite direction. The recombination shows that the electrons move from the conduction band to valence band and they emits electromagnetic energy in the form of photons. The energy of photons is equal to the gap between the valence and the conduction band. **LCD:** The LCD is defined as the diode that uses small cells and the ionised gases for the production of images. The LCD works on the modulating property of light. **Construction&Working**	04 M 04M 04M

Simple facts that should be considered while making an LCD:

1.The basic structure of the LCD should be controlled by changing the applied current.

2.We must use polarized light.

3.The liquid crystal should able be to control both of the operations to transmit or can also able to change the polarized light.



As mentioned above that we need to take two polarized glass pieces filter in the making of the liquid crystal. The glass which does not have a polarized film on the surface of it must be rubbed with a special polymer that will create microscopic grooves on the surface of the polarized glass filter. The grooves must be in the same direction as the polarized film.

Now we have to add a coating of pneumatic liquid phase crystal on one of the polarizing filters of the polarized glass. The microscopic channel causes the first layer molecule to align with filter orientation. When the right angle appears at the first layer piece, we should add a second piece of glass with the polarized film. The first filter will be naturally polarized as the light strikes it at the starting stage.

Thus the light travels through each layer and guided to the next with the help of a molecule. The molecule tends to change its plane of vibration of the light to match its angle. When the light reaches the far end of the liquid crystal substance, it vibrates at the same angle as that of the final layer of the molecule vibrates. The light is allowed to enter into the device only if the second layer of the polarized glass matches with the final layer of the molecule.

How LCDs Work?

The principle behind the LCDs is that when an electrical current is applied to the liquid crystal molecule, the molecule tends to untwist. This causes the angle of light which is passing through the molecule of the polarized glass and also causes a change in the angle of the top polarizing filter. As a result, a little light is allowed to pass the polarized glass through a particular area of the LCD.

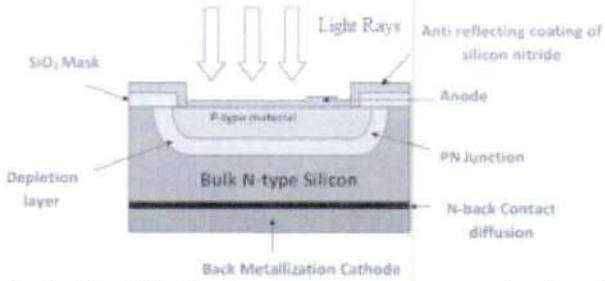
Thus that particular area will become dark compared to others. The LCD works on the principle of blocking light. While constructing the LCDs, a reflected mirror is arranged at the back. An electrode plane is made of indium-tin-oxide which is kept on top and a polarized glass with a polarizing film is also added on the bottom of the device. The complete region of the LCD has to be enclosed by a common electrode and above it should be the liquid crystal matter.

Photo diode: A special type of PN junction device that generates current when exposed to light is known as Photodiode. It is also known as photodetector or photosensor. It operates in reverse biased mode and converts light energy into electrical energy

Construction&Working

The photodiode construction can be done using two semiconductors like P-type & N-type. In this design, the formation of P-type material can be done from the diffusion of the P-type substrate which is lightly doped. So, the P+ ions layer can be formed because of the diffusion method. On the substrate of N-type, the N-type

epitaxial layer can be grown.

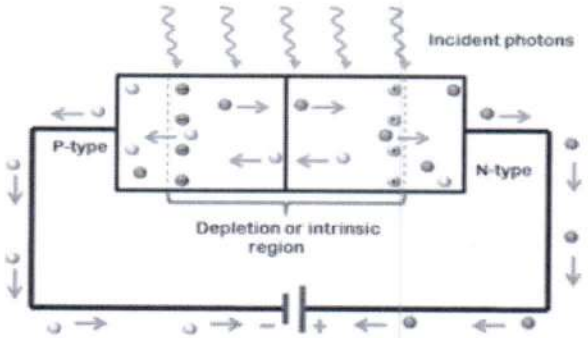


The development of a P+ diffusion layer can be done over the heavily doped N-type epitaxial layer. The contacts are designed with metals to make two terminals like anode and cathode. The front region of the diode can be separated into two types like active & non-active surfaces.

The designing of the non-active surface can be done with silicon dioxide (SiO2). On an active surface, the light rays can strike over it whereas, on a non-active surface, the light rays cannot strike. & the active surface can be covered through the material of anti-reflection so that the energy of light cannot lose and the highest of it can be changed into the current.

Working of Photodiode

The working principle of a photodiode is, when a photon of ample energy strikes the diode, it makes a couple of an electron-hole. This mechanism is also called the inner photoelectric effect. If the absorption arises in the depletion region junction, then the carriers are removed from the junction by the inbuilt electric field of the depletion region.

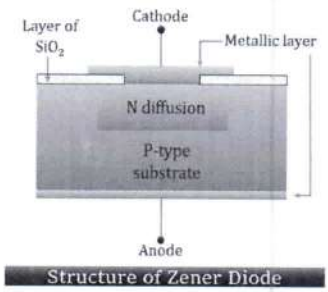


Therefore, holes in the region move toward the anode, and electrons move toward the cathode, and a photocurrent will be generated. The entire current through the diode is the sum of the absence of light and the photocurrent. So the absent current must be reduced to maximize the sensitivity of the device.

OR

b(i) A special type of PN junction diode that operates in reverse biased mode, more specifically in breakdown region is known as Zener Diode. 04M

Construction:



Structure of Zener Diode

Working of Zener diode

The operation of a zener diode is like a normal diode in forward biased mode.
However, a zener shows variation from a normal diode in the aspect of its doping concentration.
Zener diode is highly doped thus its depletion width is very thin. Due to this, more current flows through a zener diode as compared to a normal junction diode.

It specifically acts in the breakdown region in the reverse biased condition. A zener diode shows two breakdown approach, zener breakdown, and avalanche breakdown.

Let us separately understand the two breakdown mechanism.

Avalanche breakdown mechanism

Avalanche breakdown is usually subjected to happen when the applied reverse bias voltage is high. As we already know that in reverse biased condition, small minority current flows through a normal diode. When a high reverse biased voltage is applied to the device, the minority carriers experience acceleration and moves with high velocity. During its movement, minority carriers collide with the atoms and generate more number of free electrons. These free electrons further generate some more free electrons. Thus, a high electric current is generated due to this multiplicative action.

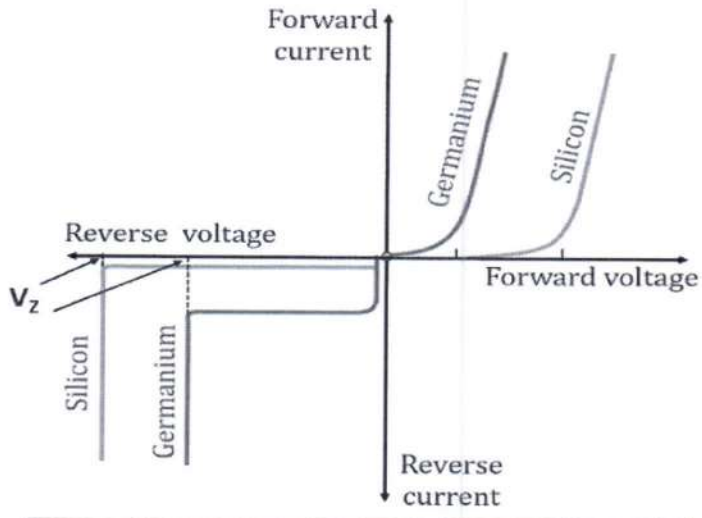
Hence, we say high potential in reverse bias is required in case of avalanche breakdown. This high current is responsible for the permanent destruction of a normal diode. But an avalanche diode carefully manufactured to operate in breakdown region withstand the high current flowing through it.

Zener breakdown mechanism

This breakdown mechanism is noticed in diodes that are heavily doped. Due to the high concentration of impurities, the width of the depletion width is narrow. With the increase in reverse potential, a strong electric field is generated by the depletion region.

As the reverse potential is supplied to the device and the voltage reaches near to zener voltage. The electrons present in the depletion region utilize that energy and get separated with the parent atom. Thereby generating free electrons. This action generates more free electrons and hence their movement produces electric current through the device. Thus, a small increase in reverse voltage will cause an immediate increase in current through the device. The current flowing through the device shows its maximal increase up to circuit permissible value. This reverse current will remain constant for a wide range of reverse potential.

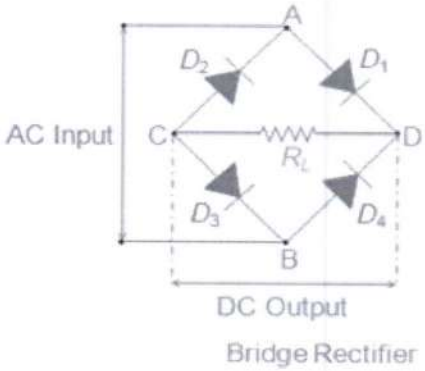
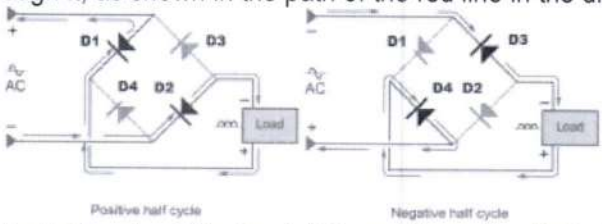
VI Characteristics of Zener Diode

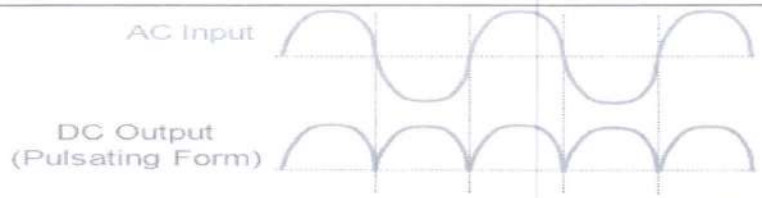


V-I characteristics of Zener Diode

The figure represents the curve for both silicon and germanium diodes. The forward characteristic of the zener diode is similar to a normal diode which is clearly seen in the figure above.

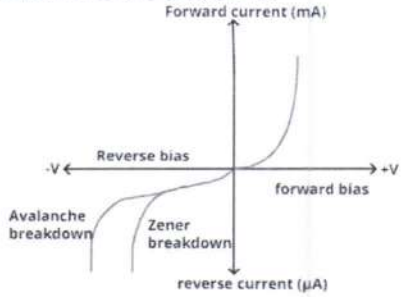
In reverse biased condition, a small reverse current flows due to minority charge carriers. On increasing the reverse voltage, current increases. A point is reached when the junction gets destroyed and a sharp increase in current is noticed without any noticeable increase in reverse potential. This voltage is known as zener voltage. The current through the device is limited by making use of external

		resistance.	
	b(ii)	**Bridge Rectifier:Construction** The bridge rectifier construction is shown below. This circuit can be designed with four diodes namely D1, D2, D3 & D4 along with a load resistor (RL). The connection of these diodes can be done in a closed-loop pattern to convert the AC (alternating current) to DC (Direct Current) efficiently. The main benefit of this design is the lack of an exclusive center-tapped transformer. So, the size, as well as cost, will be reduced. Once the input signal is applied across the two terminals like A & B then the o/p DC signal can be attained across the RL. Here load resistor is connected in between two terminals like C & D. The arrangement of two diodes can be made in such a way that the electricity will be conducted by two diodes throughout every half cycle. The pairs of diodes like D1& D3 will conduct electric current throughout the positive half cycle. Similarly, D2 & D4 diodes will conduct electric current throughout a negative half cycle.  Bridge Rectifier **Bridge Rectifier Operation** As we discussed above, a single-phase bridge rectifier consists of four diodes and this configuration is connected across the load. For understanding the bridge rectifier's working principle, we have to consider the below circuit for demonstration purposes. During the Positive half cycle of the input AC waveform diodes, D1 and D2 are forward biased and D3 and D4 are reverse biased. When the voltage, more than the threshold level of the diodes D1 and D2, starts conducting – the load current starts flowing through it, as shown in the path of the red line in the diagram below.  Positive half cycle Negative half cycle During the negative half cycle of the input AC waveform, the diodes D3 and D4 are forward biassed, and D1 and D2 are reverse biased. Load current starts flowing through the D3 and D4 diodes when these diodes start conducting as shown in the figure. We can observe that in both cases, the load current direction is the same, i.e., up to down as shown in the figure – so unidirectional, which means DC current. Thus, by the usage of a bridge rectifier, the input AC current is converted into a DC current. The output at the load with this bridge wave rectifier is pulsating in nature, but producing a pure DC requires an additional filter like a capacitor. The same operation is applicable for different bridge rectifiers, but in the case of controlled rectifiers thyristors triggering is necessary to drive the current to load. Wave forms:	04M



Input-Output Waveforms of a Bridge Rectifier

b(iii) **Zener Breakdown vs Avalanche break down:**



1.The Zener breakdown can be defined as the flow of electrons across the p kind material barrier of the valence band to the evenly filled n-type material conduction band. 04M
2.The avalanche breakdown is an occurrence of raising the flow of electric current or electrons in insulating material or semiconductor by giving the high voltage.
3.The depletion region of the Zener is thin whereas the avalanche is thick.
4.The connection of the Zener is not-destroy whereas the avalanche is destroyed.
5.The electric field of the Zener is strong whereas the avalanche is weak.
6.The Zener breakdown generates electrons whereas the avalanche generates holes as well as electrons.

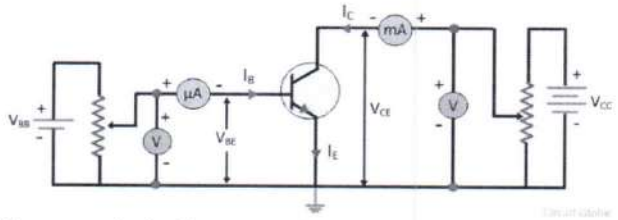
UNIT-III

3 a(i) **Definition:** The configuration in which the emitter is connected between the collector and base is known as a common emitter configuration

In common emitter configuration, base is the input terminal, collector is the output terminal and emitter is the common terminal for both input and output. That means the base terminal and common emitter terminal are known as input terminals whereas collector terminal and common emitter terminal are known as output terminals.

In common emitter configuration, the emitter terminal is grounded so the common emitter configuration is also known as grounded emitter configuration. Sometimes common emitter configuration is also referred to as CE configuration, common emitter amplifier, or CE amplifier. The common emitter (CE) configuration is the most widely used transistor configuration. 06 M

Circuit:



Input Characteristic Curve and output characteristic curve

The common emitter (CE) amplifiers are used when large current gain is needed.

The input signal is applied between the base and emitter terminals while the output signal is taken between the collector and emitter terminals. Thus, the emitter terminal of a transistor is common for both input and output and hence it is named as common emitter configuration.

In common emitter (CE) configuration, input current or base current is denoted by IB and output current or collector current is denoted by IC.

The common emitter amplifier has medium input and output impedance levels. So the current gain and voltage gain of the common emitter amplifier is medium. However, the power gain is high.

To fully describe the behavior of a transistor with CE configuration, we need two set of characteristics – input characteristics and output characteristics.

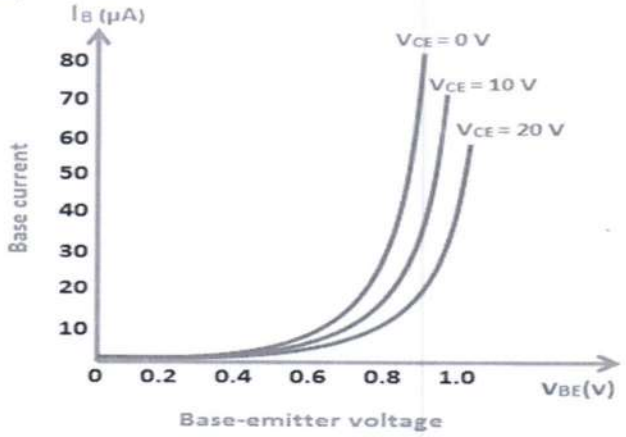
The supply voltage between base and emitter is denoted by VBE while the supply voltage between collector and emitter is denoted by VCE.

Input characteristics

The input characteristics describe the relationship between input current or base current (IB) and input voltage or base-emitter voltage (VBE).

First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The input current or base current (IB) is taken along y-axis (vertical line) and the input voltage (VBE) is taken along x-axis (horizontal line).

To determine the input characteristics, the output voltage VCE is kept constant at zero volts and the input voltage VBE is increased from zero volts to different voltage levels. For each voltage level of input voltage (VBE), the corresponding input current (IB) is recorded.



I/P characteristics CE configuration

A curve is then drawn between input current IB and input voltage VBE at constant output voltage VCE (0 volts).

Next, the output voltage (VCE) is increased from zero volts to certain voltage level (10 volts) and the output voltage (VCE) is kept constant at 10 volts. While increasing the output voltage (VCE), the input voltage (VBE) is kept constant at zero volts. After we kept the output voltage (VCE) constant at 10 volts, the input voltage VBE is increased from zero volts to different voltage levels. For each voltage level of input voltage (VBE), the corresponding input current (IB) is recorded.

A curve is then drawn between input current IB and input voltage VBE at constant output voltage VCE (10 volts).

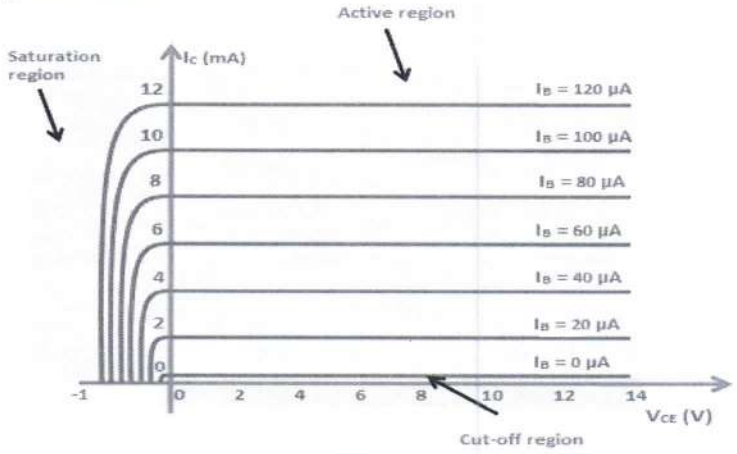
This process is repeated for higher fixed values of output voltage (VCE).

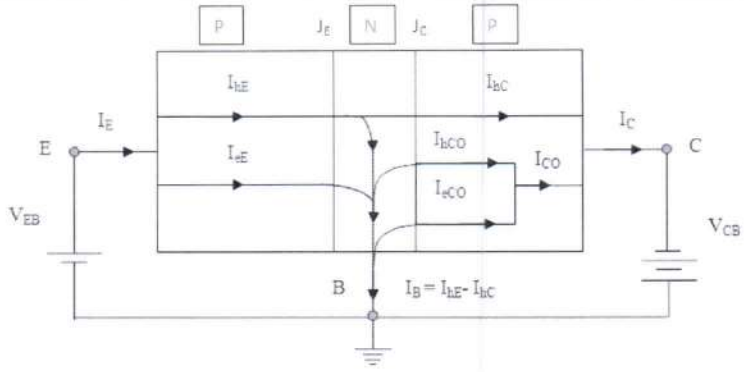
When output voltage (VCE) is at zero volts and emitter-base junction is forward biased by input voltage (VBE), the emitter-base junction acts like a normal p-n junction diode. So the input characteristics of the CE configuration is same as the characteristics of a normal pn junction diode.

The cut in voltage of a silicon transistor is 0.7 volts and germanium transistor is 0.3 volts. In our case, it is a silicon transistor. So from the above graph, we can see that after 0.7 volts, a small increase in input voltage (VBE) will rapidly increases the input current (IB).

In common emitter (CE) configuration, the input current (IB) is very small as compared to the input current (IE) in common base (CB) configuration. The input current in CE configuration is measured in microamperes (μA) whereas the input current in CB configuration is measured in milliamperes (mA).

In common emitter (CE) configuration, the input current (IB) is produced in the base region which is lightly doped and has small width. So the base region produces only a small input current (IB). On the other hand, in common base (CB) configuration, the input current (IE) is produced in the emitter region which is heavily doped and has large width. So the emitter region produces a large input current (IE).

		Therefore, the input current (IB) produced in the common emitter (CE) configuration is small as compared to the common base (CB) configuration. Due to forward bias, the emitter-base junction acts as a forward biased diode and due to reverse bias, the collector-base junction acts as a reverse biased diode. Therefore, the width of the depletion region at the emitter-base junction is very small whereas the width of the depletion region at the collector-base junction is very large. If the output voltage VCE applied to the collector-base junction is further increased, the depletion region width further increases. The base region is lightly doped as compared to the collector region. So the depletion region penetrates more into the base region and less into the collector region. As a result, the width of the base region decreases which in turn reduces the input current (IB) produced in the base region. From the above characteristics, we can see that for higher fixed values of output voltage VCE, the curve shifts to the right side. This is because for higher fixed values of output voltage, the cut in voltage is increased above 0.7 volts. Therefore, to overcome this cut in voltage, more input voltage VBE is needed than previous case. **Output characteristics** The output characteristics describe the relationship between output current (IC) and output voltage (VCE). First, draw a vertical line and a horizontal line. The vertical line represents y-axis and horizontal line represents x-axis. The output current or collector current (IC) is taken along y-axis (vertical line) and the output voltage (VCE) is taken along x-axis (horizontal line). To determine the output characteristics, the input current or base current IB is kept constant at 0 µA and the output voltage VCE is increased from zero volts to different voltage levels. For each level of output voltage, the corresponding output current (IC) is recorded.  O/P Characteristics CE Configuration A curve is then drawn between output current IC and output voltage VCE at constant input current IB (0 µA). When the base current or input current IB = 0 µA, the transistor operates in the cut-off region. In this region, both junctions are reverse biased. Next, the input current (IB) is increased from 0 µA to 20 µA by adjusting the input voltage (VBE). The input current (IB) is kept constant at 20 µA.	
a(ii)		**Transistor current components:** The conduction of current in NPN transistor is owing to electrons and in PNP transistor, it is owing to holes. The direction of current flow will be in opposite direction. Here, we can discuss the current components in a PNP transistor with common base configuration. The emitter-base junction (JE) is forward biased and the collector-base junction (JC) is reversed biased as shown in figure. All the current components related to this transistor are shown here.	06M



Explanation

We know that, the current arrives the transistor through the emitter and this current is called emitter current (I_E). This current consists of two constituents – Hole current (I_{hE}) and Electron current (I_{eE}). I_{eE} is due to passage of electrons from base to emitter and I_{hE} is due to passage of holes from emitter to base.

$$I_E = I_{hE} + I_{eE}$$

Normally, the emitter is heavily doped compared to base in industrial transistor. So, the Electron current is negligible compared to Hole current. Thus we can conclude that, the whole emitter current in this transistor is due to the passage of holes from the emitter to the base.

Some of the holes which are crossing the junction J_E (emitter junction) combines with the electrons present in the base (N-type). Thus, every holes crossing J_E will not arrive at J_C. The remaining holes will reach the collector junction which produces the hole current component, I_{hC}. There will be bulk recombination in the base and the current leaving the base will be

$$I_B = I_{hE} - I_{hC}$$

The electrons in the base which are lost by the recombination with holes (injected into the base across J_E) are refilled by the electrons that enter into the base region. The holes which are arriving at the collector junction (J_C) will cross the junction and it will go into the collector region.

When the emitter circuit is open circuited, then $I_E = 0$ and $I_{hC} = 0$. In this condition, the base and collector will perform as reverse biased diode. Here, the collector current, I_C will be same as reverse saturation current (I_{CO} or I_{CBO}).

I_{CO} is in fact a small reverse current which passes through the PN junction diode. This is due to thermally generated minority carriers which are pushed by barrier potential. This reverse current increase; if the junction is reverse biased and it will have the same direction as the collector current. This current attains a saturation value (I_0) at moderate reverse biased voltage.

When the emitter junction is at forward biased (in active operation region), then the collector current will become

$$I_C = \alpha I_E + I_{CO}$$

The α is the large signal current gain which is a fraction of the emitter current which comprises of I_{hC}.

When the emitter is at closed condition, then $I_E \neq 0$ and collector current will be

$$I_C = I_{CO} + I_{hC}$$

In a PNP transistor, the reverse saturation current (I_{CBO}) will comprises of the current due to the holes passing through the collector junction from the base to collector region (I_{hCO}) and the current due to the electrons which are passing through the collector junction in the opposite direction (I_{eCO}).

$$Therefore,\ I_{CO} = I_{hCO} + I_{eCO}$$

The total current entering into the transistor will be equal to the total current leaving the transistor (according to Kirchhoff's current law).

$$So,\ I_E = I_C + I_B\ or\ I_E = -(I_C + I_B)$$

OR

b(i) The alpha factor (**α**) of a transistor is the ratio of its collector and emitter currents (**α =**

		Ic/Ie), and it is always less than 1 (between 0.5 and 1). The beta (**β**) or current gain is the ratio of its collector and base currents (**β = Ic/Ib**), and it is always more than 1. The **α** factor is also calculated as **α = β/(β+1)** **β** can be calculated from **α** this way: **β = α/(1-α)** Current Amplification Factor (**γ**) : The ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B) is known as Current Amplification factor in common collector (CC) configuration. Current Amplification Factor (**γ**) = **β +1**	06M
	b(ii)		06M

Parameter	Common Base	Common Emitter	Common Collector
Voltage Gain	High, Same as CE	High	Less than Unity
Current Gain	Less than Unity	High	High
Power Gain	Moderate	High	Moderate
Phase inversion	No	Yes	No
Input Impedance	Low (50 Ohm)	Moderate (1 KOhm)	High (300 KOhm)
Output Impedance	High (1 M Ohm)	Moderate (50 K)	Low (300 Ohm)

UNIT-IV

4 a(i) **Thermal Runaway:** The problem with increasing temperature causing increasing collector current is that more current increase the power dissipated by the transistor which, in turn, increases its temperature. This self-reinforcing cycle is known as thermal run away, which may destroy the transistor. 06M

Stability Factor (S): The rate of change of collector current w.r.to the collector leakage current (I_{CBO} or I_{Co}) is called stability factor (S).

$$S = \left.\frac{dI_c}{dI_{co}}\right|_{\beta, I_B = \text{constant}} \quad \text{——— (a)}$$

→ Lower the value of S, better is the thermal stability of the transistor.

Expression for stability factor:

we have $I_C = \beta I_B + (1+\beta) I_{CO}$

differentiating w.r.to I_C, we get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta)\frac{dI_{Co}}{dI_C}$$

$$1 = \beta \cdot \frac{dI_B}{dI_C} + (1+\beta)\left(\frac{1}{S}\right)$$

$$\frac{(1+\beta)}{S} = 1 - \beta \frac{dI_B}{dI_C}$$

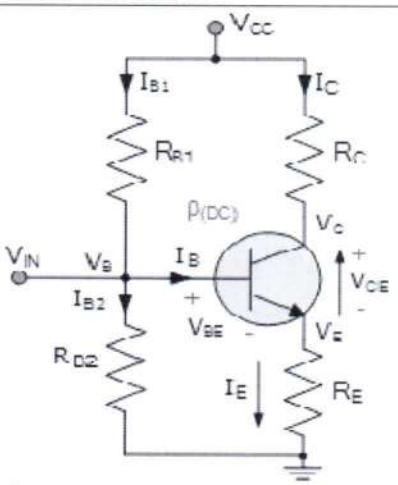
$$S\left(1 - \beta \frac{dI_B}{dI_C}\right) = (1+\beta)$$

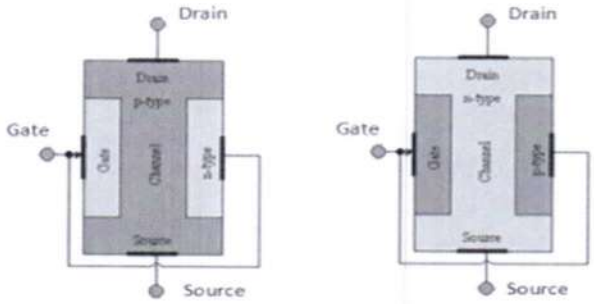
(or)

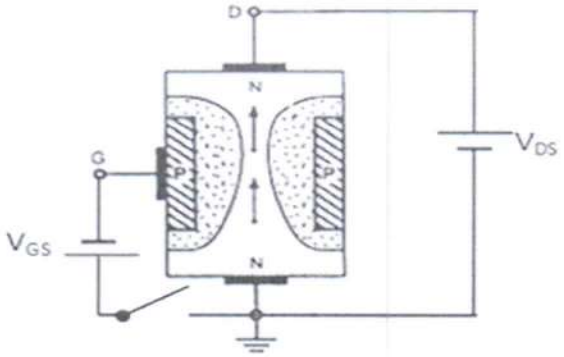
$$\boxed{S = \frac{1+\beta}{1-\beta\frac{dI_B}{dI_C}}}$$

//

a(ii) In fixed bias, V_{cc}=9v, R_c=3kΩ, R_b=8kΩ, β=50 and V_{BE}=0.7V

		$I_{c(sat)} = \frac{Vcc}{Rc}$ =3mA $V_{ce(sat)} = V_{cc}$ Operating point Q(V_{ce} ,I_c) =(4.5V,1.5mA) Stability Factor S=1+β=51	06M
		OR	
	b(i)	**Transistor Biasing:** Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor **Need of biasing:** 1.if a transistor is to operate as a linear amplifier, it must be properly biased to have a suitable operating point. 2.Establishing the correct operating point requires the proper selection of bias resistors and load resistors to provide the appropriate input current and collector voltage conditions. 3.The correct biasing point for a bipolar transistor, either NPN or PNP, generally lies somewhere between the two extremes of operation with respect to it being either "fully-ON" or "fullyOFF" along its load line **Types of bias circuits:** 1. Fixed bias 2. Collector-to-base bias 3. Fixed bias with emitter resistor 4. Voltage divider bias or potential divider 5. Emitter bias	06M
	b(ii)	 $V_C = V_{CC} - R_C I_C = (V_E + V_{CE})$ $V_C = I_C R_C = V_D - V_{DC}$ $V_{CE} = V_C - V_E = V_{CC} - (I_C R_C + I_E R_E)$ $V_B = V_{BE} + V_E = V_{RB2} = \left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right) V_{CC}$ $I_{B2} = \frac{V_B}{R_{B2}}$ $I_{B1} = I_B + I_{B2} = \frac{V_{CC} - V_B}{R_{B1}}$ $R_B = \frac{R_{B1} \times R_{B2}}{R_{B1}+R_{B2}}$ $I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta)R_E}$ $I_C = \beta_{(DC)} I_B$ $I_E = I_C + I_B = \frac{V_E}{R_E}$ **Voltage Divider Explanation** Here the common emitter transistor configuration is biased using a voltage divider network to increase stability. The name of this biasing configuration comes from the fact that the two resistors RB1 and RB2 form a voltage or potential divider network across the supply with their center point junction connected the transistors base terminal as shown. This voltage divider biasing configuration is the most widely used transistor biasing method. The emitter diode of the transistor is forward biased by the voltage value developed across resistor RB2. Also, voltage divider network biasing makes the transistor circuit independent of changes in beta as the biasing voltages set at the transistors base, emitter, and collector terminals are not dependant on external circuit values. To calculate the voltage developed across resistor RB2 and therefore the voltage applied to the base terminal we simply use the voltage divider formula for resistors in series. Generally the voltage drop across resistor RB2 is much less than for resistor RB1. Clearly the transistors base voltage VB with respect to ground, will be equal to the voltage across RB2. The amount of biasing current flowing through resistor RB2 is generally set to 10 times the value of the required base current IB so that it is sufficiently high enough to have no effect on the voltage divider current or changes in Beta.	06M

		The goal of Transistor Biasing is to establish a known quiescent operating point, or Q-point for the bipolar transistor to work efficiently and produce an undistorted output signal. Correct DC biasing of the transistor also establishes its initial AC operating region with practical biasing circuits using either a two or four-resistor bias network. In bipolar transistor circuits, the Q-point is represented by (VCE, IC) for the NPN transistors or (VEC, IC) for PNP transistors. The stability of the base bias network and therefore the Q-point is generally assessed by considering the collector current as a function of both Beta (β) and temperature. Here we have looked briefly at five different configurations for "biasing a transistor" using resistive networks. But we can also bias a transistor using either silicon diodes, zener diodes or active networks all connected to the transistors base terminal. We could also correctly bias the transistor from a dual voltage power supply if so wished.	
		UNIT-V	
5	a(i)	**Definition**: JFET is the shortened form for **J**unction **F**ield **E**ffect **T**ransistor. It is a 3 terminal **semiconductor device** in which current conduction takes place only due to the flow of majority charge carriers. Thus, it is a **unipolar transistor**.JFET is a **voltage controlled device** as here the potential applied at the gate terminal controls the drain current. The current conduction is controlled by means of an electric field between the gate and the conducting channel of the device. **Construction:** A JFET consists of a p-type or n-type silicon bar containing two pn junctions at the sides as shown in fig.1.  The bar forms the conducting channel for the charge carriers. If the bar is of p-type, it is called p-channel JFET as shown in fig.1(i) and if the bar is of n-type, it is called n-channel JFET as shown in fig.1(ii). The two pn junctions forming diodes are connected internally and a common terminal called gate is taken out. Other terminals are source and drain taken out from the bar as shown in fig.1. Thus a JFET has three terminals such as , gate (G), source (S) and drain (D). The source and the drain terminals are interchangeable. The following points may be noted: 1.The input circuit (i.e. gate to source) of a JFET is reverse biased. This means that the device has high input impedance. 2.The drain is so biased w.r.t. source that drain current ID flows from the source to drain. 3.In all JFETs, source current IS is equal to the drain current i.e IS = ID. ***Working of JEFT*** The working of JFET can be explained as follows: **Case-i:** When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero as shown in fig.3(i), the two pn junctions at the sides of the bar establish depletion layers.	06 M

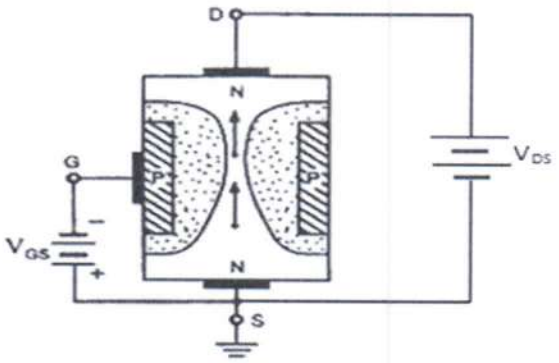


The electrons will flow from source to drain through a channel between the depletion layers.

The size of the depletion layers determines the width of the channel and hence current conduction through the bar.

Case-ii:

When a reverse voltage VGS is applied between gate and source terminals, as shown in fig.3(ii), the width of depletion layer is increased.



This reduces the width of conducting channel, thereby increasing the resistance of n-type bar.

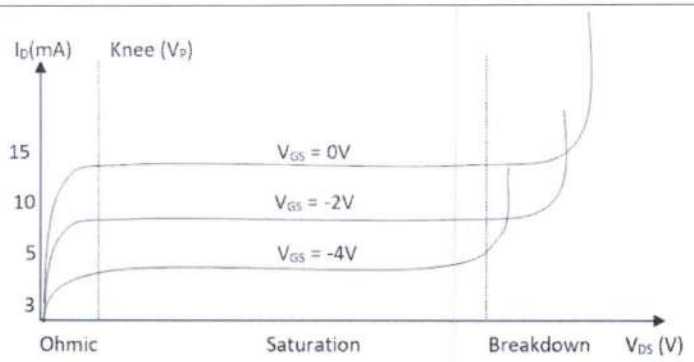
Consequently, the current from source to drain is decreased.

On the other hand, when the reverse bias on the gate is decreased, the width of the depletion layer also decreases.

This increases the width of the conducting channel and hence source to drain current.

A p-channel JFET operates in the same manner as an n-channel JFET except that channel current carriers will be the holes instead of electrons and polarities of VGS and VDS are reversed.

JFET Characteristics Curve:



a(ii) **Definition:** A solid state-operated device with the four-layered structure, its flow of current in the one direction just like a diode where it has three junctions along with the three terminals.

Working/Operation of SCR:

The basic working principle in the SCR is that as the triggering or the biasing is applied at the terminal gate then the conduction begins.

SCR triggering is a method of making the device to turn ON. It needs to be applied with a sufficient amount of biasing to the terminal gate. Hence it is known as SCR triggering. Finally as the device moves to ON state or the conducting state, the maximum amount of the current flows through the terminal anode

06M

Working or Modes of Operation of SCR

Depending on the biasing given to the SCR, the operation of SCR is divided into three modes. They are

Forward blocking Mode
Forward Conduction Mode and
Reverse Blocking Mode

Forward Blocking Mode

In this mode of operation, the Silicon Controlled Rectifier is connected such that the anode terminal is made positive with respect to cathode while the gate terminal kept open. In this state junctions J1 and J3 are forward biased and the junction J2 reverse biased.

Due to this, a small leakage current flows through the SCR. Until the voltage applied across the SCR is more than the break over voltage of it, SCR offers a very high resistance to the current flow. Therefore, the SCR acts as a open switch in this mode by blocking forward current flowing through the SCR as shown in the VI characteristics curve of the SCR.

Forward Conduction Mode

In this mode, SCR or thyristor comes into the conduction mode from blocking mode. It can be done in two ways as either by applying positive pulse to gate terminal or by increasing the forward voltage (or voltage across the anode and cathode) beyond the break over voltage of the SCR.

Once any one of these methods is applied, the avalanche breakdown occurs at junction J2. Therefore the SCR turns into conduction mode and acts as a closed switch thereby current starts flowing through it.

Note that in the VI characteristic figure, if the gate current value is high, the minimum will be the time to come in conduction mode as Ig3 > Ig2 > Ig1. In this mode, maximum current flows through the SCR and its value depends on the load resistance or impedance.

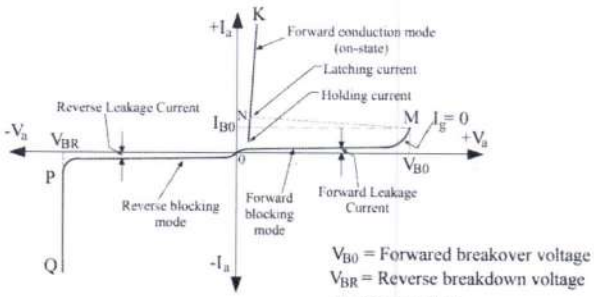
It is also noted that if gate current is increasing, the voltage required to turn ON the SCR is less if gate biasing is preferred. The current at which the SCR turns into conduction mode from blocking mode is called as latching current (IL).

And also when the forward current reaches to level at which the SCR returns to blocking state is called as holding current (IH). At this holding current level, depletion region starts to develop around junction J2. Hence the holding current is slightly less than the latching curre

Reverse Blocking Mode

In this mode of operation, cathode is made positive with respect to anode. Then the junctions J1 and J3 are reverse biased and J2 is forward biased. This reverse voltage drives the SCR into reverse blocking region results to flow a small leakage current through it and acts as an open switch as shown in figure.
So, the device offers a high impedance in this mode until the voltage applied is less than the reverse breakdown voltage VBR of the SCR. If the reverse applied voltage is increased beyond the VBR, then avalanche breakdown occurs at junctions J1 and J3 which results to increase reverse current flow through the SCR

Typical V-I Characteristics of SCR:



OR

b(i) **Construction of n-channel E-MOSFET**

Its gate construction is similar to that of D-MOSFET.

The E-MOSFET has no channel between source and drain. The substrate extends completely to the SiO2 layer so that no channel exists.

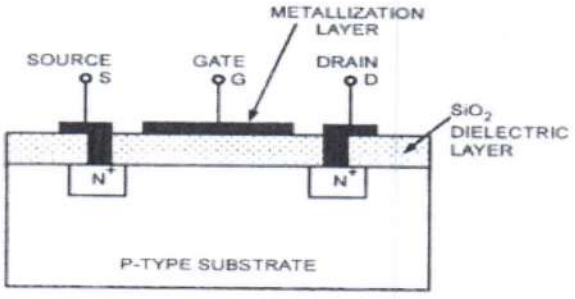
The E-MOSFET requires a proper gate voltage to form a channel , called induced channel between the source and the drain.

It operates only in the enhancement mode and has no depletion mode.

Only by applying V_{GS} of proper magnitude and polarity, the device starts conducting. 06M

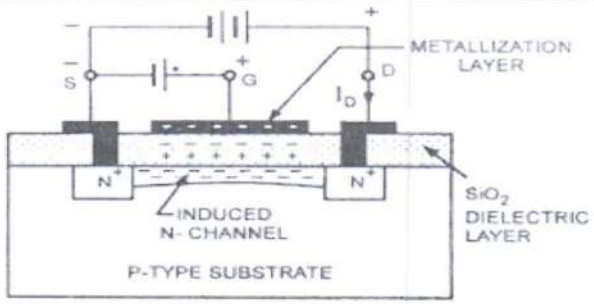
The minimum value of V_{GS} of proper polarity that turns on the E-MOSFET is called *threshold voltage* [$V_{GS(th)}$].

The n-channel device requires positive V_{GS} ($\geq V_{GS(th)}$) and the p-channel device requires negative V_{GS}($\geq V_{GS(th)}$).



N-Channel E-MOSFET Structure

Working:



Operation of N-Channel E-MOSFET

(i) **When V_{GS}= 0V,** as shown in fig.9 (i), there is no channel connecting source and drain.

The p-substrate has only a few thermally produced free electrons(minority carriers) so that drain current is almost zero. For this reason, E-MOSFET is normally OFF when V_{GS} = 0V.

(ii) **When V_{GS} is positive**, i.e gate is made positive as shown in fig.9(ii), it attracts free electrons into the p region. The free electrons combine with the holes next to the SiO2 layer.

If V_{GS} is positive enough, all the holes touching the SiO2 layer are filled and free electrons begin to flow from the source to drain.

The effect is same as creating a thin layer of n-type material i.e. inducing a thin n-layer adjacent to the SiO2 layer.

Thus the E-MOSFET is turned ON and drain current I_D starts flowing from the source to the drain.

The minimum value of V_{GS} that turns the E-MOSFET ON is called threshold voltage[$V_{GS(th)}$].

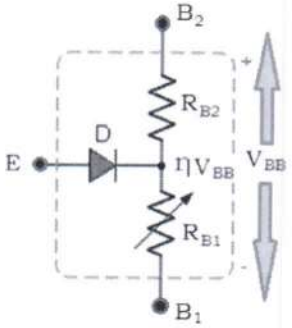
(iii) **When V_{GS} is less than $V_{GS(th)}$**, there is no induced channel and the drain current I_D is zero.

When V_{GS} is equal to $V_{GS(th)}$, the E-MOSFET is turned ON and the induced channel conducts drain current from the source to the drain.

Beyond $V_{GS(th)}$, if the value of V_{GS} is increased,the newly formed channel becomes wider, causing to I_D to increase.

If the value of V_{GS} decreases not less than $V_{GS(th)}$, the channel becomes narrower and I_D will decrease.

b(ii) **UJT Characteristics:**



06M

The variable resistance RB1 is provided between the terminals Emitter (E) and Base 1 (B1), the RB2 between the terminals Emitter (E) and Base 2 (B2). Since the PN junction is more close to B2, the value of RB2 will be less than the variable resistance RB1

A voltage divider network is formed by the series resistances RB2 and RB1. When a voltage is applied across the semiconductor device, the potential will be in proportion to the position of base points along the channel.

The Emitter (E) will act as input when employed in a circuit, as the terminal B1 will be grounded. The terminal B2 will be positive biased to B1, when a voltage (VBB) applied across the terminals B1 and B2. When the emitter input is zero, the voltage across resistance RB1 of the voltage divider circuit is calculated by

$$VRB1 = \frac{RB1}{RB1 + RB2} * VBB$$

The important parameter of Unijunction Transistor is 'intrinsic stand-off ratio' (η), which is resistive ratio of R_{B1} to R_{BB}. Most UJT's have η value ranging from 0.5 to 0.8. The PN junction is reverse biased; when small amount of voltage which is less than voltage developed across resistance R_{B1} (ηV_{BB}) is applied across the terminal emitter (E).

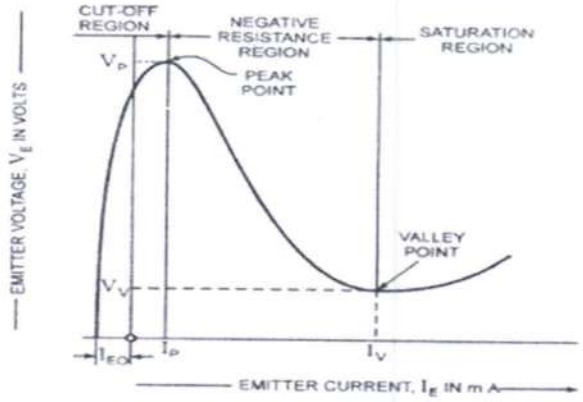
Thus a very high impedance is developed prompting device to move into non-conducting state i.e., it will be switched off and no current flows through it. The UJT begins to conduct when the PN junction is forward biased.

The forward biased is achieved when voltage applied across emitter terminal is increased and becomes more than VRB1. This results in larger flow of emitter current from emitter region to base region. Increase in emitter current reduces the resistance between emitter and Base 1, resulting in negative resistance at emitter terminal

The Unijunction Transistor (UJT) will act as voltage breakdown device, when the input applied between emitter and base 1 reduces below breakdown value i.e., RB1 increases to a higher value. This shows that RB1 depends on the emitter current and it is variable.

The characteristics of Unijunction Transistor (UJT) can be explained by three parameters:

1.Cutoff
2.Negative Resistance Region
3.Saturation



Static Emitter-Characteristic For a UJT

When the transistor reaches the triggering voltage, V_{TRIG}, Unijunction Transistor (UJT) will turn on. After a certain time, if the applied voltage increases to the emitter lead, it will reach out at V_{PEAK}. The voltage drops from V_{PEAK} to Valley Point even though the current increases (negative resistance).

Faculty Incharge

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Unit wise important questions

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Name of the Subject : Electronic Devices And Circuits (19BEC3TH02)
Year/Sem :II/I **Regulation**-R19 **Academic Year**: 2020-21

Unit Wise Important Questions

S NO	QUESTION	KNOWLEDGE LEVEL	CO
	UNIT I		
1	**List the PN diode** capacitances and solve capacitance for transition capacitance	**K4**	**CO1**
2	**Analyze** the Energy band Diagram of PN junction Diode.	**K4**	**CO1**
3	**Solve** the thermal voltage and barrier voltage at 250C , a Si PN junction is formed from P-material doped with 1022acceptors/m3 and n-material doped with 1.5 × 1021donors/m3 .	**K3**	**CO1**
4	**Analyze** VI characteristics of PN diode with Forward and Reverse bias.	**K4**	**CO1**
	UNIT 2		
1	**Analyze** Zener breakdown and Avalanche breakdown with briefly.	**K4**	**CO2**
2	**Analyze** the construction and working of LED.	**K4**	**CO2**
3	**Solve** the transformer secondary voltage for a capacitor input filter using a capacitance of 10p.F for a Full wave rectifier supplies a load requiring 300V at 200mA.	**K3**	**CO2**
4	**Analyze** the V-I Characteristic of Tunnel diode and explain its operation.	**K4**	**CO2**
	UNIT 3		
1	**Compare** α, β and γ of a transistor and also derive the relation among these.	**K4**	**CO3**
2	**Analyze** current components of transistor.	**K4**	**CO3**
3	**Solve** the IC ,IB ,β, and ICEO for a silicon, with α=0.995 emitter current is 10mA & leakage current IC0=0.5μA.	**K3**	**CO3**
4	**Compare** CB, CE & CC cofigurations.	**K4**	**CO3**
	UNIT 4		
1	**List** the advantage and disadvantages of fixed bias method.	**K4**	**CO4**
2	**Analyze** the working of collector – Base bias circuit using NPN transistor. Derive the equation for IB	**K4**	**CO4**
3	**Compare** the d.c and a.c load lines with suitable diagrams	**K4**	**CO4**

4	**Analyze** the working of Self Bias circuit using NPN transistor.	**K4**	**CO4**
	UNIT 5		
1	**Define** the Pinch-off voltage Vp. Sketch the depletion region before and after Pinch-off.	**K1**	**CO5**
2	**Explain** V-I characteristics of SCR with sketches?	**K2**	**CO5**
3	**Explain** briefly drain characteristics of N-channel enhancement MOSFET	**K2**	**CO5**
4	**Outline** the drain characteristics of a n-channel JFET and Explain it.	**K2**	**CO5**

RESULTS

RESULTS

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Name of the Subject : Electronic Devices And Circuits (19BEC3TH02)
Year/Sem :II/I **Regulation**-R19 **Academic Year**: 2020-21

END SEMESTER – RESULTS

2019 BATCH-II B.TECH I SEM -REGULAR RESULTS- AFTER REVALUATION-MARCH 2021

BRANCH : ECE

S.NO.	HTNO	STUDENT NAME	19BEC3TH02 ELECTRONIC DEVICES AND CIRCUITS		
			GR	GP	CR
1	18471A0462	ANNAM VAMSI KRISHNA	F	0	0
2	18471A04M0	VIPPARLA ARUN KUMAR	D	6	3
3	19471A0401	ALA VAMSI KRISHNA	F	0	0
4	19471A0402	ALAKUNTA RAMESH	D	6	3
5	19471A0403	AURANGABAD MAHESH GOPI	D	6	3
6	19471A0404	BATCHU MAHESH	D	6	3
7	19471A0405	CHALLAPALLI VENKATA SAI NAVEEN KUMAR	C	7	3
8	19471A0406	CHERUKURI NIKHITHESWARI	C	7	3
9	19471A0407	CHERUKURI SRINIVASA RAO	D	6	3
10	19471A0408	CHEVURI AMARESWARI	C	7	3
11	19471A0409	CHIRAMPALLI YUVA SAI	F	0	0
12	19471A0410	CHITTA TEJA SRI	C	7	3
13	19471A0411	DINDU LOKESH	D	6	3
14	19471A0412	DUGGEMPUDI SRI BHAKTHANJANEYA	D	6	3
15	19471A0413	EMANI GAYATHRI	D	6	3
16	19471A0414	GADE RAJYALAKSHMI	C	7	3
17	19471A0415	GADIPARTHI KAVITHA	C	7	3
18	19471A0416	GANTA ASHOK REDDY	D	6	3
19	19471A0417	GOTTAM HARSHAVARDHAN REDDY	F	0	0
20	19471A0418	GUDDETI VENKATESWARLU	C	7	3
21	19471A0419	GUDIPATI ASHOK KUMAR	D	6	3

22	19471A0420	GUDIPUDI GOPI	E	5	3
23	19471A0421	GUNTURU VIJAYALAKSHMI	D	6	3
24	19471A0422	KOMMANABOYINA VENKATESWARLU	D	6	3
25	19471A0423	KODAVANDLA CHANDU	E	5	3
26	19471A0424	KONDAVETI JAHNAVI	D	6	3
27	19471A0425	KONDEBOINA LAKSHMI NARAYANA	C	7	3
28	19471A0426	KONDEDDULA SWATHI	B	8	3
29	19471A0429	MADDULA VENKATESWARLU	E	5	3
30	19471A0430	MAILA TIRUPATHI	D	6	3
31	19471A0431	MANDAPATI TIRUPATHI RAO	AB	0	0
32	19471A0432	MARLAPATI KIRAN KUMAR	F	0	0
33	19471A0433	MARTHALA SAI SWETHA	C	7	3
34	19471A0434	MARURI PRIYANKA	B	8	3
35	19471A0435	NANDALA PRAVEEN	F	0	0
36	19471A0436	NOOKALA NAVEEN KUMAR	F	0	0
37	19471A0437	ORCHU SAI SIVA SATHVIKA	F	0	0
38	19471A0438	PAMARTHI VENKATA SUBRAHMANYA CHARI	E	5	3
39	19471A0439	PANGULURI SRI MANI DEEP	C	7	3
40	19471A0440	PONDUGULA BHARGAV REDDY	F	0	0
41	19471A0441	PUPPALA VENKATA SIVA SAI GOPICHAND	C	7	3
42	19471A0442	SANNEBOINA VENKATA HARI	E	5	3
43	19471A0443	SHAIK ARSHAD ALI	E	5	3
44	19471A0444	SHAIK MABU SUBHANI	C	7	3
45	19471A0445	SHAIK MOHAMMAD ALI	F	0	0
46	19471A0446	SHAIK MOHAMMAD RAFFI	C	7	3
47	19471A0447	SHAIK SAIDU BABU	B	8	3
48	19471A0448	SHAIK SHAZIAH BANU	C	7	3
49	19471A0449	SIKHINAM VENKATA RAMANJANEYULU	F	0	0
50	19471A0450	SINGAMREDDY AMARNADH REDDY	D	6	3
51	19471A0451	SINKA GOWRI SANKAR SRINIVAS	E	5	3
52	19471A0452	SOMISETTY MADHU RAMYA SAI	B	8	3
53	19471A0453	SUNKARA SRI LAKSHMI TULASI	B	8	3
54	19471A0454	TANIPARTHI HARICHANDANA	F	0	0
55	19471A0455	THOKALA TWINKLE	D	6	3
56	19471A0456	TULAVA GOPI	D	6	3
57	19471A0457	VALLEM ESWARSAI KUMAR	D	6	3

58	19471A0458	VANGAVOLU DEEPTHI	B	8	3
59	19471A0459	VARRA HARINI REDDY	D	6	3
60	19471A0460	YAMPARALA GOPI	D	6	3
61	19471A0461	AKASH REDDY BADE	D	6	3
62	19471A0462	ANNAPUREDDY PARAMESWARA REDDY	D	6	3
63	19471A0463	APPANABOINA GOPI KRISHNA	E	5	3
64	19471A0464	ARAVAPALLI HITESH LAKSHMAN KUMAR	D	6	3
65	19471A0465	ATMAKURI RAMASAI	C	7	3
66	19471A0466	BADDEPOGU RAMYA	B	8	3
67	19471A0467	BALLARI SWARUP KUMAR	F	0	0
68	19471A0468	BEERAM ANUSHA	C	7	3
69	19471A0469	BEJJANKI HARI PRASAD	F	0	0
70	19471A0470	BELLAMKONDA ARUN KUMAR	D	6	3
71	19471A0471	CHEVULA JAYASRI	D	6	3
72	19471A0472	DARA VISHNUVARDHAN	D	6	3
73	19471A0473	DIVVELA BALA LAKSHAMANA SADA SIVA	E	5	3
74	19471A0474	GADE HARIKA	D	6	3
75	19471A0475	GATTUPALLI SAI SASANK	E	5	3
76	19471A0476	GONUGUNTLA VYSHNAVI	D	6	3
77	19471A0477	GOSULA AMARA BHARGAVI	C	7	3
78	19471A0478	GUDI REVANTH KUMAR	F	0	0
79	19471A0479	GUTTIKONDA TANUJA	D	6	3
80	19471A0480	JAGARLAMUDI SAI POOJA	B	8	3
81	19471A0481	KAMEPALLI SRI VENKATA JAYA KRISHNA	E	5	3
82	19471A0482	KARNATI MANI GOPINADH	B	8	3
83	19471A0483	KATURI KISHORE	D	6	3
84	19471A0484	KOMIRI ANAND BABU	E	5	3
85	19471A0485	KONDAPALLI SIVADURGA	E	5	3
86	19471A0486	MARAMREDDY RAKESH REDDY	E	5	3
87	19471A0487	MEKALA LAKSHMI	D	6	3
88	19471A0488	MEKAPOTHULA SRINADH	F	0	0
89	19471A0489	MUDIYALA NITHIN REDDY	E	5	3
90	19471A0490	MUNNA NARENDRA	D	6	3
91	19471A0491	MUNNANGI UMA MAHESWARA REDDY	E	5	3
92	19471A0492	MUTUKURI ARUN KUMAR	E	5	3
93	19471A0493	NALLAGORLA GOPI	E	5	3

94	19471A0495	NIMMAKAYALA NAVEEN	D	6	3
95	19471A0496	PALAPARTHI PHANINDRA	E	5	3
96	19471A0497	PENDYALA MAHESH KUMAR	E	5	3
97	19471A0498	POTHABATHINI NAGA SARATH KUMAR	D	6	3
98	19471A0499	POTLA VENEELA	C	7	3
99	19471A04A0	RAJA RAJYALAKSHMI AKSHAYA	C	7	3
100	19471A04A1	RAJARAPU SAMPADA	D	6	3
101	19471A04A2	RAKESH YAMPARALA	E	5	3
102	19471A04A3	SAMPATHI SRIKANTH	E	5	3
103	19471A04A4	SHAIK ABDUL RAHAMAN	D	6	3
104	19471A04A5	SHAIK AMANULLA	F	0	0
105	19471A04A6	SHAIK INAMUL HUSSEN	E	5	3
106	19471A04A7	SHAIK KHATIB MAHAMMAD ABBAS	D	6	3
107	19471A04A8	SHAIK MUSARATH FARHANA	B	8	3
108	19471A04A9	SHAIK SAMEER BASHA	E	5	3
109	19471A04B0	SHAIK TANVEER SUHEERA	C	7	3
110	19471A04B1	SYED HUSSAINBI	C	7	3
111	19471A04B2	TAMMISETTY NITISH KUMAR	E	5	3
112	19471A04B3	THOTA SAI TEJA	C	7	3
113	19471A04B4	VAMSI KRISHNA BIKKI	C	7	3
114	19471A04B5	VEJENDLA MAHESH GOPAL	C	7	3
115	19471A04B6	VEMULURI HEMANTH	D	6	3
116	19471A04B7	VENKATA SANDHYA SYAMALA	C	7	3
117	19471A04B8	VUYYURU REVANTH	D	6	3
118	19471A04B9	YARAGALLA JAYAKANTH	C	7	3
119	19471A04C0	YARRAMREDDY JAYA SRI	B	8	3
120	19471A04C1	ACHANALA GOPINATH	E	5	3
121	19471A04C2	ADURI AMULYA	B	8	3
122	19471A04C3	AMBATI SUBRAMANYAM	B	8	3
123	19471A04C4	ANNA RAKESH	C	7	3
124	19471A04C5	ARIGELA KRISHNA BALAJI	F	0	0
125	19471A04C6	ATTHOTA MANI KUMAR	F	0	0
126	19471A04C7	BALUSUPATI CHIRANJEEVI	D	6	3
127	19471A04C8	BANDI PRIYANKA	E	5	3
128	19471A04C9	BODDULURI YOGA ALEKHYA	B	8	3
129	19471A04D0	BURRI VENKATA NAGA GOPI	E	5	3

130	19471A04D1	BUSA GNANESWAR	D	6	3
131	19471A04D2	CH MANI KUMAR	E	5	3
132	19471A04D3	CHINTHALACHERUVU VENKATESH	C	7	3
133	19471A04D4	CHUKKA ANOOP	F	0	0
134	19471A04D5	DERANGULA VIJAYA BHASKAR	D	6	3
135	19471A04D6	DEVANABOINA HEMANTH	D	6	3
136	19471A04D7	DODDA SRI VENKATA GOPAL REDDY	F	0	0
137	19471A04D8	GAJJALA UJWALA	C	7	3
138	19471A04D9	GARNEPUDI SUMANTH	E	5	3
139	19471A04E0	GUDIBANDLA SIVA RAMA KRISHNA REDDY	C	7	3
140	19471A04E1	GULLA VAMSI	F	0	0
141	19471A04E2	JADDA YEDUKONDALU	C	7	3
142	19471A04E3	JAJULA SIVA TEJA	E	5	3
143	19471A04E4	JALLI JOHN SAMUEL	D	6	3
144	19471A04E5	JAMMOJU VENU GOPALACHARI	D	6	3
145	19471A04E6	JUPUDI AJAY KUMAR	F	0	0
146	19471A04E7	KANKANALA DEVI AJAY SRINIVAS	F	0	0
147	19471A04E8	KARUMANCHI SAI KIRAN	D	6	3
148	19471A04E9	KASARAGADDA JAGADEESH	C	7	3
149	19471A04F0	KESANAPALLI JYOTHIRMAI	D	6	3
150	19471A04F1	KOKKERA PAVAN KUMAR	F	0	0
151	19471A04F2	KONJETI SRIKANTH	D	6	3
152	19471A04F4	KORNE NAGA GOPI	E	5	3
153	19471A04F5	KOSANAM UDAY KRISHNA CHAITANYA	C	7	3
154	19471A04F6	KOTHA SNEHA SATHVIKA	B	8	3
155	19471A04F7	KOYYA APARNA	C	7	3
156	19471A04F8	KSHATRI RAGHU CHANDAN SINGH	E	5	3
157	19471A04F9	MADINETI MAHESH KUMAR	E	5	3
158	19471A04G0	MANDA KOTESWARA RAO	F	0	0
159	19471A04G1	MANDALANEEDI SAIPRAVEEN	D	6	3
160	19471A04G2	MUPPURI PAVAN KUMAR	C	7	3
161	19471A04G3	NARU VISHNU PRIYA	D	6	3
162	19471A04G4	POLEBOINA SUBBA RAO	D	6	3
163	19471A04G5	PUPPALA VENKATA GANESH	D	6	3
164	19471A04G6	PUSAPATI VIGNA NARAYAN NAVEEN KUMAR REDDY	C	7	3
165	19471A04G7	RAGHUVU VENKATA TRINADH	D	6	3

166	19471A04G8	SATTENAPALLI GOPI	MP	0	0
167	19471A04G9	SAYYAD KARISHMA	C	7	3
168	19471A04H0	SEELAM TIRUPATI KOTI REDDY	C	7	3
169	19471A04H1	SHAIK ATHIKA PARVEEN	E	5	3
170	19471A04H2	SHAIK DARIYAVALI	F	0	0
171	19471A04H3	SHAIK GALIB BASHA	F	0	0
172	19471A04H4	SHAIK MAHAMMAD RAFI	F	0	0
173	19471A04H5	SHAIK RESHMA	C	7	3
174	19471A04H6	SHAIK SAMEER	F	0	0
175	19471A04H7	SHAIK UMAR	F	0	0
176	19471A04H8	SURE ESWAR PRASAD	E	5	3
177	19471A04H9	VAJRALA GOUTHAMI	D	6	3
178	19471A04I0	VAJRALA NAVEENA	C	7	3
179	19471A04I1	AASAM VIJAYA LAKSHMI	C	7	3
180	19471A04I2	ALLA MASTAN RAO	C	7	3
181	19471A04I3	ANJANEYULU DEVARASETTY	E	5	3
182	19471A04I4	ARUMULLA RAMAKANTH	C	7	3
183	19471A04I5	BONTHA VENKATA RANGA REDDY	C	7	3
184	19471A04I6	BONTHALAKOTI ATCHYUTH	C	7	3
185	19471A04I7	CHILAKALA LAKSHMI NAGA PRASANTH	E	5	3
186	19471A04I8	CHILUKURI SAI PUJITHA	B	8	3
187	19471A04I9	DASARI JANAKI VENKATESH	E	5	3
188	19471A04J0	DOKKA RAMESH	F	0	0
189	19471A04J1	DUDIPALLI SRINIVASA RAO	F	0	0
190	19471A04J2	GANDHAM SAI GOPINADH	C	7	3
191	19471A04J3	GOLLAPUDI MANI PRASAD	D	6	3
192	19471A04J4	GONUGUNTLA PRAANI PRADHAN	E	5	3
193	19471A04J5	GORU TARUN NAGA SAI	D	6	3
194	19471A04J6	ILAM VENKATA BHARGAVA	D	6	3
195	19471A04J7	INAKOLLU LAKSHMI NEELIMA	C	7	3
196	19471A04J8	JALAGAM DEVI	B	8	3
197	19471A04J9	JAMMUGANI KARTHEEK	D	6	3
198	19471A04K0	KOLLURU VENKAT RAO	C	7	3
199	19471A04K1	KOMMANABOYINA RAJESH	F	0	0
200	19471A04K2	KONDRAMUTLA MAHESH RAO	D	6	3
201	19471A04K3	KOVURI SNEHALATHA	D	6	3

202	19471A04K4	KURUVELLA VENKATESH	E	5	3
203	19471A04K5	LANKEMALLA LAKSHMAIAH	D	6	3
204	19471A04K6	MOGILI AJAYKUMAR	D	6	3
205	19471A04K7	MUDIGARLA ANUHYA	C	7	3
206	19471A04K8	NALLAGATLA SREEJA	C	7	3
207	19471A04K9	NANDAM VEERA RAGHAVULU	F	0	0
208	19471A04L0	NARRA VENKATESWARLU	D	6	3
209	19471A04L1	NARU GOPI REDDY	F	0	0
210	19471A04L2	PALLAPURAJA	D	6	3
211	19471A04L3	PASUNURI SAGAR	E	5	3
212	19471A04L4	PERAVALI BHANU AYYAPPA	E	5	3
213	19471A04L5	POGUNULLA NAGANJANEYULU	E	5	3
214	19471A04L6	POTLURI VENKATA SAI KUMAR	F	0	0
215	19471A04L7	S SHARIQA	C	7	3
216	19471A04L8	SHAIK BAJI	C	7	3
217	19471A04L9	SHAIK KARISHMA	D	6	3
218	19471A04M0	SHAIK KHALEEL REHAMAN	D	6	3
219	19471A04M1	SHAIK MASTAN SHARIEF	D	6	3
220	19471A04M2	SHAIK NAGOOR MEERAVALI	F	0	0
221	19471A04M3	SHAIK SADHIK ALLABHAKSHU	F	0	0
222	19471A04M4	SONTI DEEPAK KUMAR	F	0	0
223	19471A04M5	UDALA NAGESWAR RAO	E	5	3
224	19471A04M6	VADRA JYOTHI	F	0	0
225	19471A04M7	VAKA NARENDRA KUMAR	C	7	3
226	19471A04M8	YADALA CHANDRA MAHESH REDDY	C	7	3
227	19471A04M9	YAKKALA ASHA	E	5	3
228	19471A04N0	THINNALURI BINDU MADHAV	E	5	3
229	19471A04N1	KONGA BRAHMA TEJA	F	0	0
230	19471A04N2	GANGULA RAVI TEJA REDDY	F	0	0
231	19471A04N3	KILARU AVINASH	F	0	0
232	19471A04N5	VELPULA ESWAR KUMAR	AB	0	0
233	19471A04N6	PONNAGANTI NARASIMHA NAIDU	F	0	0
234	20475A0401	NEELISETTY KOMALI	C	7	3
235	20475A0402	PALADUGU ESWAR	D	6	3
236	20475A0403	LINGALA GRACE	A	9	3
237	20475A0404	ANUSHA BOLLA	C	7	3

238	20475A0405	DEVARAPALLI PRASANTHI	A	9	3
239	20475A0406	ELLA SRINIVAS	C	7	3
240	20475A0407	VEMULAKONDA PAVAN MANIKANTA KUMAR	B	8	3
241	20475A0408	NANDYALA JAGADEESH	C	7	3
242	20475A0409	KATTAMURI LAKSHMI PRASANNA	C	7	3
243	20475A0410	SANKULA KUSUMA	C	7	3
244	20475A0411	KOCHARLA RAMYA	B	8	3
245	20475A0412	DULAM HARSHAVARDHAN	C	7	3
246	20475A0413	VELPULA RAVIKUMAR	C	7	3
247	20475A0414	GUNJI SATYANARAYANA	C	7	3
248	20475A0415	PAYARDHA SAGAR BABU	E	5	3
249	20475A0416	YAKKALA YOGA LAKSHMI	C	7	3
250	20475A0417	DHARANI DEVI GARIKAPATI	C	7	3
251	20475A0418	ANDE SIREESHA	C	7	3
252	20475A0419	TIRUMALASETTI NIHARIKA	C	7	3
253	20475A0420	NAMPALLI AMRUTHA	D	6	3
254	20475A0421	SANGAM HENA GRACE	B	8	3
255	20475A0422	BOLLISETTY LEELA SRINIVASA KUMAR	C	7	3
256	20475A0423	NAGINENI NARENDRA	C	7	3
257	20475A0424	BANDARU VAMSI KRISHNA	E	5	3
258	20475A0425	VALAJIPETA DEVA KRISHNA SUMANTH	C	7	3
259	20475A0426	THATIKOLA GANESH	D	6	3

CHIEF CONTROLLER OF EXAMINATIONS

Previous University Question Papers

Narasaraopeta Engineering College (Autonomous)
Kotappakonda Road, Yellamanda (P.O), Narasaraopet- 522601, Guntur District, AP.

Subject Code: R16EE2102

II B.Tech I Semester Supple Examinations, October-2020

ELECTRONIC DEVICES AND CIRCUITS

(EEE)

Time: 3 hours **Max Marks: 60**

Question Paper Consists of **Part-A** and **Part-B.**

Answering the question in **Part-A** is Compulsory & Four Questions should be answered from Part-B

All questions carry equal marks of 12.

PART-A

1. (a) Explain the concept of mobility in semiconductors?
   (b) Draw the V-I characteristics of diode in forward and reverse bias?
   (c) Write the applications of Varactor diode?
   (d) Draw the input and output characteristics of common base and common emitter configuration?
   (e) What is the significance of operating point in transistors?
   (f) Define drain resistance and amplification factor in FET?

[2+2+2+2+2+2]

PART-B

4 X 12 = 48

2. (a) Explain in detail about Drift and Diffusion current? (6M)
   (b) State and explain the phenomenon of Hall Effect? (6M)

3. (a) Derive the expression for diode current equation? (6M)
   (b) Explain the mechanism of breakdown in PN junction diode? (6M)

4. (a) Derive the expression for ripple factor, efficiency and form factor of half-wave rectifier? (6M)
   (b) Explain the construction and operation of tunnel diode? (6M)

5. (a) Explain how transistor is used as a switch? (6M)
   (b) Briefly explain the concept of early effect in transistor? (6M)

6. (a) What is the need of biasing in transistors? (6M)
   (b) Explain the operation of Fixed-bias technique? (6M)

7. (a) With the neat sketches explain the operation of depletion mode MOSFET? (6M)
   (b) Explain the construction and operation of UJT? (6M)

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Narasaraopeta Engineering College (Autonomous)

KotappakondaRoad, Yellamanda (P.O), Narasaraopet- 522601, Guntur District, AP.

Subject Code: R16EE2102

II B.Tech I Semester Regular and Supplementary Examinations, November-2018.

ELECTRONIC DEVICES AND CIRCUITS

(EEE)

Time: 3 hours **Max Marks: 60**

Question Paper Consists of **Part-A** and **Part-B.**

Answering the question in **Part-A** is Compulsory & Four Questions should be answered **from Part-B**

All questions carry equal marks of 12.

PART-A

1. (a) Define intrinsic and extrinsic semiconductors.
   (b) Write diode current equation and explain about the reverse saturation current.
   (c) Give the theoretical values for ripple factor and efficiency of bridge rectifier.
   (d) What is early effect?
   (e) Define the stability factor and thermal runaway.
   (f) List the applications of UJT

[2+2+2+2+2+2]

PART-B

4 X 12 = 48

2. (a) Explain the semiconductors, insulators and metals classification using energy band diagrams. [6M]
   (b) Explain the principle of Hall Effect with diagram and write its applications [6M]

3. (a) Explain the working of PN junction diode in forward and reverse bias conditions. [6M]
   (b) Derive an expression for Transition and Diffusion capacitances of a PN junction diode? [6M]

4. (a) Explain the construction and working of Tunnel diode.
   (b) Explain the construction and working of LCD. [6M]

5. (a) Explain input and output characteristics of common emitter configuration. [8M]
   (b) Compare CE, CB and CC configurations [4M]

6. (a) What is Biasing? Explain the need of it? List the different types of biasing methods. [6M]
   (b) Derive an expression for stability factor of self-bias circuit. [6M]

7. (a) Explain in detail the working of JFET and draw its drain and transfer characteristics. [6M]
   (b) Explain about Construction, Operation and Characteristics of UJT? [6M]

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Narasaraopeta Engineering College (Autonomous)

Kotappakonda Road, Yellamanda (P.O), Narasaraopet- 522601, Guntur District, AP.

Subject Code: R16EC2102

II B.Tech I Semester Supplementary Examinations, May-2018.

ELECTRONIC DEVICES AND CIRCUITS

(ECE)

Time: 3 hours **Max Marks: 60**

Question Paper Consists of **Part-A** and **Part-B.**

Answering the question in **Part-A** is Compulsory & Four Questions should be answered from Part-B

All questions carry equal marks of 12.

PART-A

1. (a) Define Mass action law.
   (b) Explain law of junction.
   (c) What is Zener breakdown?
   (d) What is early effect in BJT?
   (e) What is thermal runaway in BJT?
   (f) Define transconductance of FET?

[2+2+2+2+2+2]

PART-B

4 X 12 = 48

2. (a) Explain quantitative analysis of Hall effect and its applications. [6 M]
   (b) Explain the Fermi level in extrinsic semiconductors. [6 M]

3. (a) Explain operation of P-N diode under forward and reverse bias using V-I characteristics.[6M]
   (b) Define static, dynamic and reverse resistance of P-N junction diode. [6 M]

4. (a) Explain the V-I characteristics of the Tunnel diode and also discuss the negative resistance of tunnel diode. [6 M]
   (b) A full wave bridge rectifier having load resistance of 800 ohms is fed with 220 V, 50 Hz through step-down transformer of turns ration 10:1. Assume ideal diodes and find peak inverse voltage and rectifier efficiency. [6 M]

5. (a) Explain input and output characteristics of Common Base configuration. [6 M]
   (b) Compare CB, CE and CC amplifiers with respect to different parameters. [6 M]

6. (a) Explain DC load line and AC load line. Also difference between them. [6 M]
   (b) Derive the condition for thermal stability of BJT used in a biasing circuit. [6 M]

7. (a) Explain working principle and characteristics of JFET. [6 M]
   (b) Explain negative resistance property of UJT and application of UJT. [6 M]

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Narasaraopeta Engineering College (Autonomous)

KotappakondaRoad, Yellamanda (P.O), Narasaraopet- 522601, Guntur District, AP.

Subject Code: R16EE2102

II B.Tech I Semester Regular Examinations, Nov-2017.

ELECTRONIC DEVICES AND CIRCUITS

(EEE)

Time: 3 hours **Max Marks: 60**

Question Paper Consists of **Part-A** and **Part-B.**

Answering the question in **Part-A** is Compulsory & Four Questions should be answered from Part-B

All questions carry equal marks of 12.

PART-A

1. (a) What are conductors, insulators and semiconductors?
   (b) What are the applications of PN junction diode?
   (c) Define Transition capacitance and Diffusion capacitance.
   (d) Define avalanche and zener breakdown mechanisms and write any two differences.
   (e) What is the need for biasing?
   (f) What are the differences between BJT and JFET?

[2+2+2+2+2+2]

PART-B

4 X 12 = 48

2. (a) Explain Fermi level in an extrinsic semiconductor with energy diagram. [8M]
   (b) With a neat sketch explain about Hall Effect. [4M]

3. (a) Derive the diode current equation. [8M]
   (b) A silicon diode has reverse saturation current of 2.5 μA at 300^{0} K. Find forward voltage for a forward current of 10mA. [4M]

4. (a) With a neat sketch explain the working of bridge rectifier. [6M]
   (b) Explain the construction and working of Photo Diode. [6M]

5. (a) Explain the input and output characteristics of transistor in common base configuration. [6M]
   (b) Define α and β and derive the relation between them. [6M]

6. (a) Draw the transistor biasing circuit using fixed bias arrangement and explain its principle with suitable analysis. [6M]
   (b) In a silicon transistor with fixed bias, V_{CC} =9V, R_C =3 kΩ, R_B =8 kΩ, β=50, V_{BE}=0.7V. Find the operating point and stability factor. [6M]

7. (a) Explain the construction and operation of depletion mode MOSFET. [6M]
   (b) Explain working of two transistor model of an SCR and Draw the SCR characteristics. [6M]

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NEC NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

II B.Tech I Semester Regular Examinations, March-2021

Sub Code: 19BEC3TH02 **ELECTRONIC DEVICES AND CIRCUITS**

Time: 3 hours (ECE) Max. Marks: 60

Note: Answer All **FIVE** Questions.

All Questions Carry Equal Marks (5 X 12 = 60M)

Q.No		Questions	Marks
1		Unit-I	
	a	i) Explain the semiconductors, insulators and metals classification using energy band	[6M]
		ii) Find the concentration of holes and electrons in a p-type germanium at 3000K, if the conductivity is 100Ω-cm. mobility of holes in germanium μp = 1800cm2 /Vsec	[6M]
		OR	
	b	i) Explain the Diffusion and Drift currents for a semiconductor	[6M]
		ii) Show that the Fermi energy level lies in the centre of forbidden energy band for an intrinsic semiconductor? Derive	[6M]
2		Unit-II	
	a	Explain the following diodes in detail (i) LED (ii) LCD (iii) Photodiode	[12M]
		OR	
	b	i) Explain the construction and working of Zener diode along with diagram	[4M]
		ii) With circuit and necessary waveforms explain the operation of bridge rectifier	[4M]
		iii) Compare and contrast Zener breakdown and Avalanche breakdown	[4M]
3		Unit-III	
	a	i) Explain input and output characteristics of common emitter configuration along with characteristics	[6M]
		ii) Explain the concept of Transistor Current Components in detail	[6M]
		OR	
	b	i) Explain the Relation among α, β, and γ in detail	[6M]
		ii) List out few comparisons of CB, CE and CC Configurations along with examples	[6M]
4		Unit-IV	
	a	i) What is thermal runaway? Derive relevant expressions to obtain thermal stability	[6M]
		ii) In a silicon transistor with a fixed bias, Vcc= 9 V, Rc= 3 kΩ, RB= 8kΩ, β = 50, V_{BE}= 0.7V. Find the operating point and stability factor	[6M]
		OR	
	b	i) What is Biasing? Explain the need of it. List out different types of biasing methods	[6M]
		ii) With the help of neat diagram explain the voltage divider biasing method for Transistor.	[6M]
5		Unit-V	
	a	i) Draw the construction diagram, operation characteristics and parameters of JFET	[6M]
		ii) Draw and explain the working operation of SCR along with characteristics	[6M]
		OR	
	b	i) Explain the construction and working of Enhancement MOSFET	[6M]
		ii)Write short notes on UJT-Negative Resistance Property in detail	[6M]

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Missing Topics(Course gaps) and Topics beyond Syllabus

NARASARAOPETA
NEC ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Name of the Subject : Electronic Devices And Circuits (19BEC3TH02)
Year/Sem :II/I **Regulation**-R19 **Academic Year**: 2020-21

TOPICS BEYOND SYLLABUS:

1. Overview of Semiconductors and Diodes
2. Knowledge on Transistors

Signature of the Faculty Incharge

Remedial/corrective actions

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

Department of ELECTRONICS & COMMUNICATION ENGINEERING

Name of the Faculty: Dr.T.Santhi
Subject: EDC
Branch: ECE

Academic Year: 2020-21
Year/Sem: II/I
Section: A, B.

S. NO	Date	Name Of The Topic	Signature of the faculty
1	9/2/2021	Diodes zener, Tunnel	T Santhi
2	16/2/2021	Transistors, (CB, CE, CC) configurations	T Santhi
3	23/2/2021	Types of Rectifiers.	T Santhi

HOD

NARASARAOPETA
NEC ENGINEERING COLLEGE
(AUTONOMOUS)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Name of the Faculty: Dr. T. Santhi,
Subject: EDC
Branch: ECE

Academic Year: 2020-2021
Year/Sem: II/I
Section: A&B

SLOW LEARNERS

S.NO	ROLL NUMBER	MARKS (MID-1)	CLASS-1 9/2/2021	CLASS-2 16/2/2021	CLASS-3 23/2/2021	CLASS-4	CLASS-5	CLASS-6	CLASS-7	CLASS-8	MARKS (MID-2)
1	19471A0409	22	Ch.Yuva Sai	Ch.Yuva Sai							17
2	19471A0417	23	G.H.Reddy		Ch.Yuvasai						18
3	19471A0431	0	M.Tirupathi Rao								0
4	19471A0432	14	M.kiran kumar	M.Kiran kumar	M.Kiran Kumar						20
5	19471A0435	2	N.Praveen	N Praveen	N.Praveen						12
6	19471A0436	16	N.Naveen kumar	N.Naveen kumar							11
7	19471A0437	15	O.Sai Siva Satvika	O.S.Siva Satvika	O.S Siva Satvika						17
8	19471A0440	6	P.Bhargav Reddy	P.Bhargav Reddy	P.Bhargav reddy						17
9	19471A0442	11	S.V.Hari	S.V.Hari	S.V Hari						18
10	19471A0449	14	S.V Ramanjaredu	Sv.Ramanjaneku	S.V ramanjaredu						18
11	19471A0455	17	T.Twinkle	T.Twinkle	T.Twinkle						25
12	19471A0467	3	B.S Kumar	B.S kumar							9
13	19471A0469	12	B.H Prasad	B.H Prasad							6
14	19471A0478	13	G.Reventh Kumar	G.Reventh Kumar	G.Reventh reddy						15
15	19471A0486	20	M.Rakesh reddy	M.rakesh reddy							18
16	19471A0496	14	P.Phanindra	P.Phanindra	P.Phanindra						19
17	19471A04A5	8	SK.Amarulla	SK.Amarula	SK.Amarula						12

Signature of the faculty

Signature of the HOD

NARASARAOPETA
NEC ENGINEERING COLLEGE
(AUTONOMOUS)

S.NO	ROLL NUMBER	MARKS (MID-1)	CLASS-1	CLASS-2	CLASS-3	CLASS-4	CLASS-5	CLASS-6	CLASS-7	CLASS-8	MARKS (MID-2)
			9/2/2021	16/2/2021	23/2/2021						
18	18471A0462	13	A.V. Krishna	A.V. Krishna							12
19	19471A04J0	19	D. Ramesh	D. Ramesh							18
20	19471A04J1	16	D.S Rao	D.S Rao							8
21	19471A04J4	14	G.P. Pradhan	G.P. Pradhan	G.P Pradhan						18
22	19471A04K1	14	K. Rajesh	K. Rajesh							5
23	19471A04L1	18	N.G. Reddy	N.G. Reddy	N.G. Reddy						23
24	19471A04L6	9	P.V. Sai Kumar	P.V. Sai Kumar							7
25	19471A04M2	11	S.N. Meeravali	S.N. Meeravali	S.N. meeravali						17
26	19471A04M4	12	S.D Kumar	S.D. Kumar	S.D. Kumar						24
27	19471A04M5	0	U.N. Rao	U.N. Rao	U.N. Rao						20
28	19471A04N1	18	K.B. Teja	K.B. Teja	K.B. Teja						20
29	19471A04N2	11	G.R.T Reddy	G.R.T. Reddy	G.R.T. Reddy						18
30	19471A04N3	18	K. Avinash	K. Avinash							12
31	19471A04N5	5	V. Eswar Kumar	V. Eswar Kumar	V. Eswar Kumar						0
32	19471A04N6	11	P.N. Naidu	P.N. Naidu	P.N. Naidu						14
33	20475A0415	5	P.S Baba	P.S. Baba	P.S. Baba						20
34	20475A0424	22	B.V. Krishna	B.V. Krishna	B.V. Krishna						27

Signature of the faculty

Signature of the HOD

NARASARAOPETA ENGINEERING COLLEGE
(AUTONOMOUS)

Department of ELECTRONICS & COMMUNICATION ENGINEERING

Name of the Faculty: P.S.S. Chakravarthy
Subject: EDC
Branch: ECE

Academic Year: 2020-21
Year/Sem: II/II
Section: C & D

S. NO	Date	Name Of The Topic	Signature of the faculty
1	9/2/2021	Special diodes (Zener, Tunnel)	
2	16/2/2021	Rectifiers	
3	23/2/2021	Transistor CB, CC configurations	

HOD