Narasaraopeta Engineering College (Autonomous)

Kotappakonda Road, Yellamanda (P.O), Narasaraopet- 522601, Guntur District, AP.
Sponsored by Gayatri Educational Development Society, Narasaraopet.
Approved by AICTE, New Delhi & Permanently affiliated to JNTUK, Kakinada. Code: 47.
Twice Accredited by NBA & NAAC with "A" Grade; ISO 9001:2008 Certified Institution.
Phone: 08647239905 Website: www.nrtenggcollege.com Email: nrtec_principal@yahoo.com

Electronics and communication Engineering Department

NEC
NARASARAOPETA
ENGINEERING COLLEGE

R19 M.Tech

ACADEMIC REGULATIONS

ACADEMIC REGULATIONS - 2019 FOR M.TECH

(Effective for the students admitted into I year from the Academic Year 2019-20 and onwards)

1. QUALIFICATION FOR ADMISSION

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit / rank obtained by the candidates at the qualifying entrance test GATE/PGECET or on the basis of any other order of merit as approved by the Government from time to time.

2. AWARD OF M.TECH. DEGREE

A student will be declared eligible for the award of the M. Tech. Degree, if he fulfils the following academic requirements.

(a) Pursue a course of study for not less than two academic years and not more than four academic years.

(b) The candidate registers for 80 credits and secure all 80 credits.

3. COURSES OF STUDY

The following courses of study are offered at present as specializations in the M.Tech. courses with English as medium of instruction.

S. No.	Specialization Code	Abbreviation
01	06 - DSCE	Digital Systems and Computer Electronics
02	15 - MD	Machine Design
03	21 - TE	Thermal Engineering
04	38 - DECS	Digital Electronics and Communication Systems
05	42 - P&ID	Power and Industrial Drives
06	58 - CSE	Computer Science and Engineering
07	87 - SE	Structural Engineering

And any other course as approved by the authorities from time to time.

4. STRUCTURE OF THE PROGRAMME

Semester	Credits
I M.TECH I SEM	21
I M.TECH II SEM	21
II M.TECH III SEM	38
II M.TECH IV SEM	
TOTAL	80

Each course is normally assigned a certain number of credits as follows:

- 3 credits for 4 lecture periods.

- 3 credits for 6 laboratory periods per week.
- 1 credit for seminar.
- 2 credits for comprehensive viva
- 35 credits for project work.

5. DISTRIBUTION AND WEIGHTAGE OF MARKS

The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks for theory / practical / seminar / comprehensive viva on the basis of internal evaluation and end semester examinations.

5.1 THEORY

All theory subjects consisting of 6 units in each subject, the assessment shall be for 40 marks through internal evaluation and 60 marks through external end semester examination of 3 hours duration.

5. 1.a. INTERNAL EVALUATION

The internal evaluation will be based on two cycle tests conducted in each semester. The 40 internal marks will be awarded as 75% of the best cycle and 25% of the least cycle examinations, where each cycle of examination contain
Descriptive test - 30 Marks
Assignment test - 10 Marks

Each descriptive test question paper contains3 questions one from each unit covering syllabus from 3 units (first 3 units for first cycle and the remaining 3 units for second cycle). The student has to answer all the three questions (3X10M=30M).The descriptive examination will be conducted for1½ hour duration.

In Assignment Tests 5 or 6 questions will be declared in the class room at least one week in advance. In the test, two questions (one from each unit) will be given at random to each student and the student has to answer it.
The Assignment Test-1 will be conducted for 10 marks covering the syllabus from 1st& 2ndunits.The Assignment Test-2 will be conducted for 10 marks from 4th& 5th units.

5.1.b. EXTERNAL EVALUATION

The question paper comprises of 8 questions, there should be one from each unit. Student has to answer 5 questions out of 8, each question carry 12marks (5X12=60). The duration of end theory examination is 3 hours.

5.2 PRACTICALS

For practical subjects evaluation is as follows during the semester

5.2.a. INTERNAL EVALUATION

There shall be continuous evaluation during the semester for 40 internal marks. The internal marks shall be awarded as follows:

Record	- 10 Marks
Day-to-day work	- 15 Marks
Internal Lab Test	- 15Marks

5.2.b. EXTERNAL EVALUATION

For practical subjects there shall be an external examination at the end of the semester for 60 marks in the presence of external examiner.

5.3 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the end semester examination and a minimum of 50% of the total marks in the end semester examination and internal evaluation taken together.

5.4 SEMINAR

For seminar, a student under the supervision of a faculty member shall collect the literature on an advanced topic related to his specialization and review the literature then submit it to the department in a report form during the third semester and shall make an oral presentation before the departmental review committee consisting of the supervisor and head of the department / a senior faculty member. There shall be an internal evaluation for 100 marks in the form of viva voce examination and assessment of report and its presentation. There will be NO external evaluation. A candidate shall be deemed to have secured the minimum academic requirement in seminar, if he secures a minimum of 50% of marks in the examination.

If a candidate fails to secure the minimum marks prescribed for successful completion, he has to re-register and he has to submit a fresh report and appear for the evaluation by the committee.

5.5 COMPREHENSIVE VIVA-VOCE

Comprehensive viva voce examination is conducted during the 3rd semester in all the subjects of first & second semesters of the course by a committee consisting of two senior faculty members of the department. There will be NO external evaluation.

A candidate shall be deemed to have secured the minimum academic requirement in seminar, if he secures a minimum of 50% of marks in the examination.

If a candidate fails to secure the minimum marks prescribed for successful completion, he has to re-register and undergo viva voce examination.

5.6 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.3) he has to re-appear for the end semester examination in that subject.

A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate is less than 50% and has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-register subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks in the previous attempt stand cancelled. For re-registration the candidates have to apply to the college by paying the requisite fee and get approval from the authorities before the beginning of the semester in which re-registration is required.

5.7 In case the candidate secures less than the required attendance in any re-registered subject(s), he shall not be permitted to write the End examination in that subject. He shall again re-register the subject when next offered.

5.8 Laboratory examinations must be conducted with two examiners, one of them being the laboratory class teacher or teacher of the respective college and the second examiner shall be appointed by the Principal from the panel of examiners submitted by the respective departments.

5.9 PROJECT WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

5.9.1. A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members.

5.9.2. Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

5.9.3. After satisfying 5.9.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval. The students can initiate the Project work, only after obtaining the approval from the Project Review Committee (PRC).

5.9.4. If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Project Review Committee (PRC). However, the Project Review Committee (PRC) shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of supervisor or topic as the case may be.

5.9.5. A candidate shall submit his status report in two stages at least with a gap of 3 months between them.

5.9.6. The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project

Thesis only after successful completion of theory and practical subjects with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical subjects before submission of the Thesis.

5.9.7. Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.

5.9.8. The thesis shall be adjudicated by one examiner selected by the authorities. For this, the HOD of the concerned dept. shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned.

5.9.9. If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is unfavourable again, the thesis shall be summarily rejected. The candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the authorities.

5.9.10. If the report of the examiner is favourable, viva-voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the thesis. The Board shall jointly report the candidate's work as one of the following: Grade O(Outstanding)/ Grade A(Excellent)/Grade B(Very Good) /Grade C(Good)/ Grade D(Pass)/ Grade F(Fail).

The Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination.

5.9.11. If the report of the viva-voce is Grade F, the candidate shall retake the viva-voce examination only after three months. If he fails to get a satisfactory report at the second viva-voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the authorities.

6. ATTENDANCE REQUIREMENTS:

(i) A student shall be eligible to appear for the end examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

(ii) Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester for genuine medical reasons and shall be approved by a committee duly appointed by the college. A fee stipulated by the college shall be payable towards condonation of shortage of attendance. However the number of condonations is restricted to two for the entire course.

(iii) A student who is short of attendance in a semester may seek re-admission into that semester when offered next time, within 4 weeks from the date of commencement of class work.

(iv) If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for re-admission into the same class.

7. COURSE PATTERN:

(i) The entire course of study is of two academic years and every year will have TWO Semesters.
(ii) A student is eligible to appear for the end examination in a subject, but absent for it or has failed in the end examinations may appear for that subject in supplementary examinations, when conducted next.
(iii) When a student is detained due to shortage of attendance, he may be re-admitted in to the same semester/year in which he has been detained.

8. METHOD FOR AWARDING OF GRADE POINTS FOR A SUBJECT:

Theory/ Laboratory / Seminar/ Comprehensive viva/ Project (% of marks in a subject)	Corresponding Grade Points	Letter Grade
91 - 100	10	O (Outstanding)
81 - 90	9	A (Excellent)
71 - 80	8	B (Very Good)
61 - 70	7	C (Good)
51 - 60	6	D (Pass)
< 50	0	F (Fail)

9. Criteria for award of grades/division.

9.1 Calculation of Semester Grade Point Average (SGPA)* for semester

The performance of each student at the end of each semester is indicated in terms of SGPA. The SGPA is calculated as given below:

$$\text{SGPA} = \frac{\sum (CR \, X \, GP)}{\sum CR}$$

Where CR= Credits of a subject
GP = Grade Points awarded for a subject
*SGPA is calculated for a candidate who passed all the subjects in that semester.

9.2 Calculation of Cumulative Grade Point Average (CGPA) for Entire Program:

The CGPA is calculated as given below:

$$\text{CGPA} = \frac{\sum (CR \, X \, GP)}{\sum CR}$$

Where CR = Credits of a subject
GP = Grade Points awarded for a subject

- The SGPA and CGPA shall be rounded off to 2 decimal point and reported in the transcripts.
- Equivalent percentage = (CGPA – 0.75) x 10

9.3 Award of Division:

After satisfying the requirements prescribed for the completion of the program, the student shall be eligible for the award of M.Tech Degree and shall be placed in one of the following classes:

CGPA	Class
≥ 7.75	First Class with Distinction (Provided all the subjects should pass in the first attempt)
≥ 6.75	First Class (with subject failures)
≥ 5.75 & < 6.75	Second Class

10. REVALUATION:

1. Student can submit the application for revaluation, along with the prescribed fee for revaluation of his answer script(s) of theory subject(s) as per the notification issued by the Controller of Examinations.

2. The Controller of Examinations shall arrange for revaluation of such answer script(s).

3. An External examiner, other than the first examiner shall revaluate the answer script(s).

11. MINIMUM INSTRUCTION DAYS:
The minimum instruction days for each semester shall be 90 working days.

12. There shall be no branch transfer after the completion of admission process.

13. WITHHOLDING OF RESULTS

If the student has not paid the dues, if any, to the college or if any case of indiscipline is pending against him, the result of such student will be kept withheld. His degree will be withheld in such cases.

14. TRANSITORY REGULATIONS

Discontinued or detained candidates are eligible for readmission as and when next offered.
A candidate, who is detained or discontinued in a semester, on readmission shall be required to do all the subjects in the curriculum prescribed for the batch of students in which the student joins subsequently. However, exemption will be given to those candidates who have already passed such subjects in the earlier semester(s) he was originally admitted into and substitute subjects are offered in place of them as decided by the Board of Studies. However, the decision of the Board of Studies will be final.

14.1 A student who is following JNTUK curriculum and detained due to shortage of attendance at the end of the first semester of first year shall join the autonomous batch of first year first semester. Such students shall study all the subjects prescribed for the batch in which the student joins and considered on par with regular candidates of Autonomous stream and will be governed by the autonomous regulations.

14.2 A student who is following JNTUK curriculum, detained due to shortage of attendance at the end of the second semester of first year or at the subsequent semesters shall join with the autonomous batch in the appropriate semester. Such candidates shall be required to pass in all the subjects in the program prescribed by the Board of Studies concerned for that batch of students from that semester onwards to be eligible for the award of degree. However, exemption will be given in the subjects of the semester(s) of the batch which he had passed earlier and substitute subjects will be offered in place of them as decided by the Board of Studies. The student has to clear all his backlog subjects up to previous semester by appearing for the supplementary examinations conducted by JNTUK for the award of degree will be sum of the credits up to previous semester under JNTUK regulations and the credits prescribed for the semester in which a candidate seeks readmission and subsequent semesters under the autonomous stream. The class will be awarded based on the academic performance of a student in the autonomous pattern.

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MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT INEXAMINATIONS

- The Principal shall refer the cases of Malpractices in Internal Assessment Test and Semester end examinations to a malpractice prevention committee constituted by him for the purpose. Such committee shall follow the approved levels of punishment. The Principal shall take necessary action against the students based on the recommendations of the committee.

- Any action by the candidate trying to get undue advantage in the performance or trying to help another, or derive the same through unfair means is punishable according to the provisions contained hereunder:

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	Nature of Malpractices/ Improper conduct	**Punishment**
	If the candidate:	
1(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination).	Expulsion from the examination hall and cancellation of the performance in that subject only.
1(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination(theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the college.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall.

		The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from classwork and all college examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from classwork and all college examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent /any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-incharge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s)has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

	in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from classwork and all college examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6to 8.	Student of the college expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the college will be handed over to police and, a police case will be registered against them.

10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the college for further action to award suitable punishment.	

OTHER MATTERS:

1. Physically challenged candidates who have availed additional examination time and a scribe during their UG / PGECET examinations will be given similar concessions on production of relevant proof / documents.

2. The Principal shall deal in an appropriate manner with any academic problem which is not covered under these rules and regulations, in consultation with the Heads of the departments and subsequently such actions shall be placed before the Academic Council for ratification. Any emergency modification of regulation, approved in the meetings of the Heads of the departments shall be reported to the Academic Council for ratification.

GENERAL:

1. The academic council may, from time to time, revise, amend or change the regulations, schemes of examinations and / or syllabi.
2. Wherever the words ‘’he’’ ‘’him’’ ‘’his’’, occur in the regulations, they include ‘’she’’, ’’her’’, ’’hers’’.
3. The academic regulation should be read as a whole for the purpose of any interpretation.
4. In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the principal is final.

COURSE STRUCTURE & SYLLABUS
FOR
M.Tech-ECE-DIGITAL SYSTEMS AND COMPUTER ELECTRONICS (DSCE)

I M.Tech-I SEMESTER

S.No.	Name of Subject	L	T	P	Internal Marks	External Marks	Total Marks	Credits
1	Digital System Design	4	-	-	40	60	100	3
2	VLSI Technology and Design	4	-	-	40	60	100	3
3	Wireless Communication and Networks	4	-	-	40	60	100	3
4	Advanced Computer Architecture	4	-	-	40	60	100	3
5	**Elective I** i. Digital Data Communications ii. Digital Design Using HDL iii. Analog and Digital IC Design iv. Internet Protocols v. Pattern Recognition	4	-	-	40	60	100	3
6	**Elective II** i. System Modelling and Simulation ii. Network Security and Cryptography iii. Image and Video Processing iv. Mobile Computing Technologies v. Algorithms for VLSI Design Automation	4	-	-	40	60	100	3
7	Design and Simulation Laboratory	-	-	6	40	60	100	3
	TOTAL	**24**	**-**	**6**	**280**	**420**	**700**	**21**

I M.Tech-II SEMESTER

S.No.	Name of Subject	L	T	P	Internal Marks	External Marks	Total Marks	Credits
1	CMOS Analog and Digital IC Design	4	-	-	40	60	100	3
2	DSP Processors and Architectures	4	-	-	40	60	100	3
3	Embedded System Design	4	-	-	40	60	100	3
4	Adhoc & Wireless Sensor Networks	4	-	-	40	60	100	3
5	**Elective III** i. System On Chip Design ii. Soft Computing Techniques iii. Cyber Security iv. Advanced Digital System Design v. Coding Theory & Applications	4	-	-	40	60	100	3
6	**Elective IV** i. Embedded Real Time Operating System ii. High Speed Networks iii. Data Communication and Networks iv. Advanced Digital Communication v. Embedded Networking	4	-	-	40	60	100	3
7	Embedded Systems Laboratory	-	-	6	40	60	100	3
	TOTAL	**24**	**-**	**6**	**280**	**420**	**700**	**21**

M.Tech-III & IV SEMESTERS

S.No.	Name Of Subject	Total Marks	Credits
1	Seminar	100	1
2	Comprehensive Viva-Voce	100	2
3	Dissertation	-	35
	TOTAL	200	**38**

I M.Tech I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS1TH01	**DIGITAL SYSTEM DESIGN**						

COURSE OBJECTIVES:

- An ability to implement minimization of switching functions in different methods and implementation of CAMP Algorithm.
- An ability to synthesize logic and state machines using a PLA design and minimization and implementation of state machines using Field-Programmable Gate Arrays, CPLDs etc.
- An ability to design a computer to be fault-tolerant for combinational circuits and sequential circuits.

COURSE OUTCOMES:

By End of this course, the students will able to

CO1: Apply the minimization of switching functions in different methods.
CO2: Implement the CAMP Algorithm.
CO3: Synthesizes the logic and state machines using a PLA design and minimization
CO4: Implement the state machines using Field-Programmable Gate Arrays.
CO5: Design a fault-tolerant for combinational and sequential circuits circuits.

UNIT-I

Introduction to Minimization Procedures: Review on minimization of switching functions using tabular methods, K-map, QM algorithm,

UNIT-II

CAMP Algorithm: CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-III

PLA Design, Minimization and Folding Algorithms: Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm (IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT -IV

Design of Large Scale Digital Systems: Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, and PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-V

Fault Diagnosis in Combinational Circuits: Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test

set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built-in-self-test.

UNIT-VI

Fault Diagnosis in Sequential Circuits: Fault detection and location in sequential circuits, circuit test approach, initial state identification, Hamming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS:

1. N. N. Biswas, "*Logic Design Theory*", PHI.
2. Z. Kohavi, "*Switching and Finite Automata Theory*", 2nd Edition, TMH, 2001.
3. Parag K. Lala, "*Digital System Design using PLDs*", PHI, 1984.

REFERENCES:

1. Charles H. Roth, "*Fundamentals of Logic Design*", 5th Ed., Cengage Learning.
2. MironAbramovici, Melvin A.Breuer andArthur D. Friedman, "*Digital Systems Testing and Testable Design*", John Wiley & Sons Inc.

I M.Tech I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MEC1TH02	**VLSI TECHNOLOGY AND DESIGN**						

COURSE OBJECTIVES:

- Able to create models of ASIC, FPGA, moderately sized CMOS circuits that realize specified digital functions.
- Able to design CMOS and BiCMOS circuits.
- Able to design a subsystem and layout.

COURSE OUTCOMES:

By End of this course, the students will able to

CO1: Apply a mathematical methods and circuit analysis models in analysis of CMOS circuits.
CO2: Create models of ASIC,FPGA that realize specified digital functions.
CO3: Apply design issues for testability.
CO4: Demonstrate the characteristics of BiCMOS circuit.
CO5: Design and draw various subsystems and layouts.
CO6: Comprehend the chip design and floor planning methods.

UNIT-I

VLSI Technology: Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.
VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT-II

CMOS VLSI Design: MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies**,** comparison of different processes.
Building Blocks of a VLSI circuit: Computer architecture, memory architectures, communication interfaces, mixed signal interfaces.

UNIT-III

VLSI Design Issues: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

UNIT-IV

Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitative and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT-V

Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.

Subsystem Design Processes: Some general considerations and an illustration of design processes, design of an ALU subsystem. 24 2013-14

UNIT-VI

Floor Planning: Introduction**,** Floor planning methods, off-chip connections.

Architecture Design: Introduction, Register-Transfer design, highlevel synthesis, architectures for low power, architecture testing.

Chip Design: Introduction and design methodologies.

TEXT BOOKS:

1. K. Eshraghian, Douglas A. Pucknell, SholehEshraghian, "*Essentials of VLSI Circuits and Systems"*, PHI Publications, 2005.

2.Wayne Wolf, *"Modern VLSI Design"*, 3rd Ed., Pearson Education, 1997.

3. Dr.K.V.K.K.Prasad, KattulaShyamala,*"VLSI Design"*, Kogent Learning Solutions Inc., 2012.

REFERENCES:

1. RandallL.Geiger, Phillip E.Allen, Noel R.Strader,*"VLSI Design Technologies for Analog and Digital Circuits"*, TMH Publications, 2010.

2. Ming-BO Lin, *"Introduction to VLSI Systems: A Logic, Circuit and System Perspective"*, CRC Press, 2011.

3. N.H.E Weste, K. Eshraghian, "*Principals of CMOS VLSI Design*", 2nd Edition, Addison Wesley.

I M.Tech I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MEC1TH06	**WIRELESS COMMUNICATIONS AND NETWORKS**						

COURSE OBJECTIVES:

- To demonstrate the concepts of basic cellular system, frequency reuse, channel assignment strategies, handoff strategies, interference.
- To comprehend the Mobile radio propagation for small scale fading and multipath, large scale path loss.
- To study the different generations of mobile networks, WAN and IEEE 802.11.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Comprehend the concepts of spectrum allocation, basic cellular system, frequency reuse, channel assignment strategies, handoff strategies, interference, improving coverage and capacity, cell splitting.
CO2: Describe the Mobile radio propagation large scale path loss.
CO3: Extent the different outdoor propagation models.
CO4: Express the mobile radio propagation for small scale fading and multipath.
CO5: Describe the different equalizers and diversity techniques.
CO6: Development of the different wireless networks.

UNIT-I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference, Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring.

UNIT–II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edgeDiffraction, Scattering.

UNIT–III

Outdoor Propagation Models: Longley- Ryce Model, Okumura Model, Hata Model, PCS Extension to HataModel, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT–IV

Mobile Radio Propagation: Small –Scale Fading and Multipath Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel-Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT -V

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non-linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm,Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Techniques-Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT -VI

Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparison of IEEE 802.11 a,b,g and n standards, IEEE 802.16and its enhancements, Wireless PANs, HiperLan, WLL.

TEXT BOOKS:

1. Theodore, S. Rappaport, "*Wireless Communications, Principles, Practice*", 2nd Ed., PHI, 2002.
2. Andrea Goldsmith, "*Wireless Communications*", Cambridge University Press, 2005.
3. GottapuSasibhushanaRao, "*Mobile Cellular Communication*", Pearson Education, 2012.

REFERENCES:

1. KavehPahLaven and P. Krishna Murthy, "*Principles of Wireless Networks*", PE, 2002.
2. KamiloFeher, "*Wireless Digital Communications*", PHI, 1999.
3. William Stallings, "*Wireless Communication and Networking*",PHI, 2003.
4. UpenDalal, "*Wireless Communication*", Oxford Univ. Press.
5. Vijay K. Gary, "*Wireless Communications and Networking*", Elsevier.

I M.Tech I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS1TH08	**ADVANCED COMPUTER ARCHITECTURE**						

COURSE OBJECTIVES:

- The course focus on computer design, pipelining, RISC instruction set.
- To introduce dynamic scheduling, different ILP software Techniques.
- To comprehend the concept of memory architecture, interconnection and intel architecture.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Explain the classes of computers and new trends and developments in computer design.
CO2: Extend the pipelining, RISC processor, cache memory performance.
CO3: Exploit the various techniques of a processors ability in instruction level parallelism (ILP) and its challenges.
CO4: Comprehend the architecture of Very large instruction word(VLIW).
CO5: Describe the concept of systematic and distributed shared memory architecture.
CO6: Extend the performance of interconnection network and intel architecture.

UNIT-I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, Measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, Classifying instruction set- Memory addressing- type and size of operands, Operations in the instruction set.

UNIT–II

Pipelines: Introduction, Basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design: Introduction, Review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT-III

Instruction Level Parallelism the Hardware Approach: Instruction- Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

UNIT-IV

ILP Software Approach: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT–V

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction; Characteristics of application domain, Systematic shared memory architecture, Distributedshared – memory architecture, Synchronization. 28 2013-14

UNIT–VI

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.

REFERENCE BOOKS:

1. Kai Hwang, Faye A.Brigs., "*Computer Architecture and Parallel Processing*",MC Graw Hill.

2. DezsoSima, Terence Fountain, Peter Kacsuk ,"*Advanced Computer Architecture – A Design Space Approach*", Pearson Ed.

I M.Tech I SEMESTER (ELECTIVE-I)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MEC1TH03	**DIGITAL DATA COMMUNICATIONS**						

COURSE OBJECTIVES:

- Introduce students to the evolution of digital modulation schemes and the concepts data communication.
- Awareness of different error correction codes, data link protocols.
- Introduction of different networks and multiple access techniques.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Explains the different digital modulation schemes.

CO2: Comprehend the different concepts of data communication.

CO3: Extend the different error correction codes.

CO4: Express the different data link protocols.

CO5: Extend the different networks and multiple access techniques.

UNIT-I

Digital Modulation Schemes: BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

UNIT-II

Basic Concepts of Data Communications, Interfaces and Modems: Data Communication Networks, Protocols and Standards, UART, USB, I2C, I2S, Line Configuration, Topology, Transmission Modes, Digital Data Transmission, DTE-DCE interface, Categories of Networks – TCP/ IP Protocol suite and Comparison with OSI model.

UNIT-III

Error Correction: Types of Errors, Vertical Redundancy Check (VRC), LRC, CRC, Checksum, Error Correction using Hamming code

UNIT-IV

Data Link Control: Line Discipline, Flow Control, Error Control **Data Link Protocols:** Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocols, Bit-Oriented Protocol, Link Access Procedures.

UNIT-V

Multiplexing: Frequency Division Multiplexing (FDM), Time Division Multiplexing (TDM), Multiplexing Application, DSL. **Local Area Networks:** Ethernet, Other Ether Networks, Token Bus, Token Ring, FDDI.

Metropolitan Area Networks: IEEE 802.6, SMDS **Switching:** Circuit Switching, Packet Switching, Message Switching. **Networking and Interfacing Devices:** Repeaters, Bridges, Routers, Gateway, Other Devices.

UNIT-VI

Multiple Access Techniques: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization, Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), Code Division Multiple Access (CDMA), OFDM and OFDMA.

TEXT BOOKS:

1. Data Communication and Computer Networking - B. A.Forouzan, 2nd Ed., 2003, TMH.
2. Advanced Electronic Communication Systems - W. Tomasi, 5th Ed., 2008, PEI.

REFERENCES:

1. Prakash C. Gupta, *"Data Communications and Computer Networks"*, PHI, 2006.
2. William Stallings, "*Data and Computer Communications*", 8th Ed. , PHI, 2007.
3. T. Housely, "*Data Communication and Tele Processing Systems*", 2nd Ed, BSP, 2008.
4. Brijendra Singh, "*Data Communications and Computer Networks*", 2nd Ed., PHI, 2005.

I M.Tech SEMESTER (ELECTIVE-I)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MEC1TH07	**DIGITAL DESIGN USING HDL**						

COURSE OBJECTIVES:

- Students will study the signals, variables, combinational logic circuit design using VHDL.
- Students must be able to design sequential logic circuit design using VHDL and digital logic circuits using Verilog HDL
- Students learn about synthesis and testing of digital logic circuit,CAD tools.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Demonstrate the use and application of signals, variables.
CO2: Demonstrates the application of combinational logic circuit design using VHDL.
CO3: Simulate sequential logic circuit described using VHDL.
CO4: Simulate digital logic circuits using Verilog HDL.
CO5: Synthesize digital circuits at several level of abstractions.
CO6: Test digital logic using CAD tools

UNIT-I

Digital Logic Design using VHDL: Introduction, designing with VHDL, design entry methods, logic synthesis , entities , architecture , packages and configurations, types of models: dataflow, behavioural, structural, signals vs. variables, generics, data types, concurrent vs. sequential statements , loops and program controls.

Digital Logic Design using Verilog HDL Introduction, Verilog Data types and Operators, Binary data manipulation, Combinational and Sequential logic design, Structural Models of Combinational Logic, Logic Simulation, Design Verification and Test Methodology, Propagation Delay, Truth Table models using Verilog.

UNIT-II

Combinational Logic Circuit Design using VHDL: Combinational circuits building blocks: Multiplexers, Decoders , Encoders , Code converters, Arithmetic comparison circuits , VHDL for combinational circuits , Adders-Half Adder, Full Adder, Ripple-Carry Adder, Carry Look-Ahead Adder, Subtraction, Multiplication.

UNIT-III

Sequential Logic Circuit Design using VHDL: Flip-flops, registers & counters, synchronous sequential circuits: Basic design steps, Mealy State model, Design of FSM using CAD tools, Serial Adder Example, State Minimization, Design of Counter using sequential Circuit approach.

UNIT-IV

Digital Logic Circuit Design Examples using Verilog HDL: Behavioral modeling , Data types, Boolean-Equation-Based behavioral models of combinational logics , Propagation delay and continuous assignments, latches and level-sensitive circuits in Verilog, Cyclic behavioral models of flip-flops and latches and Edge detection, comparison of styles for behavioral model; Behavioral model, Multiplexers, Encoders and Digital Systems & Computer Electronics 33Decoders, Counters, Shift Registers, Register files, Dataflow models ofa linear feedback shift register, Machines with multi cycle operations, ASM and ASMD charts for , Design examples, Keypad scanner and encoder.

UNIT-V

Synthesis of Digital Logic Circuit Design: Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic with latches and flip-flops, Synthesis of Explicit and Implicit State Machines, Registers and counters.

UNIT-VI

Testing of Digital Logic Circuits and CAD Tools: Testing of logic circuits, fault model, complexity of a test set, path-sensitization, circuits with tree structure, random tests, testing of sequential circuits, built in self test, printed circuit boards, computer aided design tools, synthesis, physical design.

TEXT BOOKS:

1. Stephen Brown &ZvonkoVranesic, "*Fundamentals of Digital logic design with VHDL*", Tata McGraw Hill,2nd edition.
2. Michael D. Ciletti, "*Advanced digital design with the Verilog HDL*", Eastern economy edition, PHI.

REFERENCES:

1. Stephen Brown &ZvonkoVranesic, "*Fundamentals of Digital logic with Verilog design*", Tata McGraw Hill,2nd edition.
2. Bhaskar, "*VHDL Primer*",3rd Edition, PHI Publications.
3. Ian Grout, "*Digital systems design with FPGAs and CPLDs*", Elsevier Publications.

I M.Tech I SEMESTER (ELECTIVE-I)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS1TH09	**ANALOG AND DIGITAL IC DESIGN**						

COURSE OBJECTIVES:

- Students will study the current mirrors and amplifiers, PLL and comparators
- Students must be able to design combinational and sequential IC design using Verilog.
- Students learn about synthesis and test D/A and A/D converters.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Describes current mirrors.
CO2: Describes current mirrors.
CO3: Design combinational logic that works.
CO4: Design sequential circuits.
CO5: Synthesize logic design Nyquist rate A/D .
CO6: Synthesize logic design Nyquist rate D/A .

UNIT-I

Current Mirrors And Single Stage Amplifiers: Simple COMS, BJT current mirror, Cascode, Wilson and Widlar current mirrors. Common Source amplifier source follower, common gate amplifier

Operational Amplifiers: General considerations one – state op-amps, two stage opamps-gains boosting stage- comparison I/P range limitations slew rate.

Phased Locked Loop Design: PLL concepts- The phase locked loop in the locked condition Integrated circuit PLLs – phase Detector- Voltage controlled oscillator case study.

UNIT-II

Comporators: Using an op-amp for a comparator-charge injection error- latched Comparator SWITHCHED CAPACITORS CIRCUITS: Basic Building blocks op-amps capacitors switches –non-over lapping clocks-Basic operations and analysis-resistor equivalence of la switched capacitor- parasitic sensitive integrator parasitic insensitive integrators signal flow graph analysis-First order filters- switch sharing fully differential filters.

UNIT-III

Combinational IC Design By Using Verilog: VERILOG modeling for decoders, encoders, multiplexers, adders and subtractors.

UNIT-IV

Sequential IC Design By Using VHD: VERILOG modeling for larches, flip flops, counters, shift registers, FSMs.

LOGIC FAMILIES & CHARACTERISTICS: COMS, TTL, ECL, logic families COMS / TTL- interfacing and comparison of logic families.

UNIT-V

Digital Integraded System Building Blocks: Multiplexers, decoders, barrel shifters, counters and digital single bit adders.

NYQUIST RATE D/A Converters: Decoder based converter resistor storing converters folded resistor string converter – Binary scale converters – Binary weighted resistor converters – Reduced resistance ratio ladders – R-2R based converters – Thermometer code current mode D/A converters.

UNIT-VI

NYQUIST RATE A/DConverters: Integrating converters – successive approximation converters. DAC based successive approximation – flash converters time interleaved A/D converters.

TEXT BOOKS:

1. David A Johns, Ken Martin, "*Analog Integrated circuit Design*", John Wiley & Sons.
2. BehzadRazavi, "*Design of Analog CMOS Integrated Circuits*", TMH
3. Ken Martin, "*Digital Integrated Circuit Design*", Oxford University, 2000
4. John F Wakerly, "*Digital Design Principles and Practices*",3rd Ed., Pearson Education & XilinxDesign Series, 2002.

REFERENCES:

1.Ken Martin, "Digital *Integrated Circuit Design*", Oxford University, 2000.
2. Samir Palnitkar, "Verylog HDL-A Guide to Digital Design and Synthesis",Prentice Hall India, 2002.

I M.Tech I SEMESTER (ELECTIVE-I)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS1TH10	**INTERNET PROTOCOLS**						

COURSE OBJECTIVES:

- Comprehend fundamental design principles of Internet Protocols, IP addressing, and IP networks, including routing and forwarding.
- Comprehend advanced Internet protocol technologies including network management, domain name system, network address translation, DHCP and multicasting.
- Application of Internet protocols to improving actual network configurations of IP routers, switches and hosts.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Describe the architecture of the Internet and able to describe IP addressing with assigned addresses.

CO2: Describe the Internet Protocol (IP) and Trans mission Control Protocol(TCP)

CO3: Describe the intra and inter routing protocols (Ex. RIP, OSPF and BGP)

CO4: Describe the Domain Name System (DNS), Network virtual terminal (NVT) and File transfer Protocol (FTP).

CO5: Comprehend of multimedia concepts.

CO6: Extend the computer networked system organization and architecture.

UNIT-I

Internetworking Concepts: Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level Interconnection, Properties of thee Internet, Internet Architecture, Wired LANS, Wireless LANs, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite.

IP Address: Classful Addressing: Introduction, Classful Addressing, Other Issues, Sub-netting and Super-netting, **Classless Addressing:** Variable length Blocks, Sub-netting, Address Allocation. Delivery, Forwarding, and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router. **ARP and RARP:** ARP, ARP Package, RARP.

UNIT–II

Internet Protocol (IP): Datagram, Fragmentation, Options, Checksum, IP V.6.

Transmission Control Protocol (TCP): TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times.

UNIT–III

Stream Control Transmission Protocol (SCTP): SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.

Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.

Classical TCP Improvements: Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/ Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP.

UNIT-IV

Unicast Routing Protocols (RIP, OSPF, and BGP): Intra and Interdomain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.

Multicasting and Multicast Routing Protocols: Unicast – Multicast Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing: MOSPF, Multicast Distance Vector: DVMRP.

UNIT –V

Domain Name System (DNS): Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet.

Remote Login TELNET: Concept, Network Virtual Terminal (NVT).

File Transfer FTP and TFTP: File Transfer Protocol (FTP).

Electronic Mail: SMTP and POP.

Network Management-SNMP: Concept, Management Components, World Wide Web-HTTP Architecture.

UNIT -VI

Multimedia: Digitizing Audio and Video, Network security, security in the internet firewalls. Audio and Video Compression, Streaming Stored Audio/Video, Streaming Live Audio/Video, Real-Time Interactive Audio/
Video, RTP, RTCP, Voice Over IP. Network Security, Security in the Internet, Firewalls.

TEXT BOOKS:

1. Behrouz A. Forouzan, "*TCP/IP Protocol Suite*", Third Edition, TMH.
2. Comer, "*Internetworking with TCP/IP*", 3rd edition PHI.

REFERENCES:

1. Mahbub Hassan, Raj Jain, "*High performance TCP/IP Networking*", PHI, 2005
2. B.A. Forouzan, "*Data Communications & Networking*", 2nd Edition, TMH
3. William Stallings, "*High Speed Networks and Internets*", Pearson Education, 2002.
4. William Stallings, "*Data and Computer Communications*", 7th Edition, PHI.
5. AdrinFarrel, "*The Internet and Its Protocols*", Elsevier, 2005.

I M.Tech I SEMESTER (ELECTIVE-I)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code:	**PATTERN RECOGNITION**						

COURSE OBJECTIVES:

- Introduce the fundamentals of statistical pattern recognition and Bayes decision theory.
- Comprehend the techniques of parameter estimation and density estimation.
- Explain the discriminant functions and clustering.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Gain idea on fundamental concepts in pattern recognition
CO2: Use the Bayesian decision theory concepts from ground level
CO3: Use the maximum likelihood estimation, Bayesian estimation in real-time applications.
CO4: Use the Non-Parametric estimation in real-time applications.
CO5: Clearly describe the Linear discriminate functions and clustering
CO6: Engage in life-long learning in the area of pattern recognition.

UNIT– I

Introduction: Machine Perception, Pattern recognition systems, the design cycle, learning and adaption.

UNIT–II

Bayesian Decision Theory: Bayesian decision theory – Continuous features, Minimum error rate classification, Classifiers, Discriminant Functions and decision surfaces, the normal density, discriminant functions for the normal density, Bayes decision theory – Discrete features.

UNIT–III

Maximum-Likelihood and Bayesian Parameter Estimation: Maximum-Likelihood Estimation, Bayesian Parameter Estimation, Bayesian Parameter Estimation: Gaussian case, Bayesian Parameter Estimation: General theory, Problems of Dimensionality, Hidden Markov Models.

UNIT–IV

Non-Parametric Techniques: Density Estimation, Parzen Windows, k_n-Nearest Neighbor Estimation, the Nearest Neighbor rule, Metrics and Nearest-Neighbor classification.

UNIT–V

Linear Discriminant Functions: Linear Discriminate Functions and decision surfaces, Generalized Linear Discriminant Functions, the two-category linearly separable case,

Minimizing the Perception criterion function, Relaxation procedures, Non-separable behavior, minimum squared-error procedures, the Ho-Kashyap procedures.

UNIT–VI

Unsupervised Learning and Clustering: Mixture densities and Identifiability, Maximum-Likelihood Estimates, Application to Normal mixtures, Unsupervised Bayesian learning, Data description and Clustering, Criterion functions for clustering, Hierarchical clustering, Component Analysis.

TEXT BOOKS:

1. Richard O. Duda, Peter E, Hart and David G. Stork, *"Pattern Classification"*, Second Edition, Wiley Publications, 2001, ISBN: 978-0-471-05669-0.

REFERENCES:

1. T.M. Mitchell, "*Machine learning*", McGraw-Hill, New York, 1997.
2. S. Theodoridis, K. Koutroumbas, *"Pattern Recognition"*, Academic Press, 1999.

I M.Tech I SEMESTER (ELECTIVE-II)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MEC1TH04	**SYSTEM MODELING AND SIMULATION**						

COURSE OBJECTIVES:

- Students will study the system models, simulators.
- Students must be able extend the probability concepts in simulation and queuing theory.
- Demonstrate about discrete system simulation, GPSS and SEMSCRIPT.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Describe, system models.
CO2: Describe, simulators.
CO3: Design probability concepts in simulation.
CO4: Design queuing theory.
CO5: Describe discrete system simulation.
CO6: Explain GPSS and SEMSCRIPT.

UNIT-I

System Models: Concepts, continuous and Discrete Systems, systems modeling, types of models, subsystems, corporate model, system study.
System simulation: Techniques, comparison of simulation and analytical methods, types of simulation, distributed log models, cobwed models.

UNIT-II

Continuous system simulation: Numerical solution of differential equations, analog computers, hybrid computers, continuous system simulation languages – CSMP, system dynamic growth models, logistic curves.

UNIT-III

Probability concepts in simulation: Monte Carlo techniques, stochastic variables, probability functions, random number generation algorithms.

UNIT-IV

Queuing Theory: Arrival pattern distribution, service times, queuing disciplines, measure of queues, mathematical solutions to queuing problems.

UNIT-V

Discrete Systems Simulation: Events generation of arrival patterns, simulation programming tasks, analysis of simulation output.

UNIT- VI

GPSS and SEMSCRIPT: General description of GPSS and SEMSCRIPT, programming in GPSS.

Simulation Programming techniques: Data Structures, implementation of activities, events and queues, event scanning, simulation algorithms in GPSS and SEMSCRIPT.

BOOKS:

1. GeofferyGordan, *"Systems Simulation"*, PHI, 1978.

I I M.Tech I SEMESTER (ELECTIVE-II)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS1TH11	**NETWORK SECURITY AND CRYPTOGRAPHY**						

COURSE OBJECTIVES:

- Comprehend the Security services and Data Encryption Algorithms.
- Recognize Cryptography Message authentication and Hash functions.
- Explain Hash Algorithms and IP security.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Explain the Security and classical encryption Techniques.
CO2: Conduct research in Network Security.
CO3: Apply Security principles in System design.
CO4: Encrypt and Decrypt the messages using Cipher Algorithms.
CO5: Use Hash and MAC algorithms in Authentication principles.
CO6: Use firewall design concepts and IP security.

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UNIT-I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

UNIT-II

Encryption Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block ciphers. **Conventional Encryption:** Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

UNIT-III

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primarily, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

UNIT-IV

Message Authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT-V

Hash and Mac Algorithms MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD- 160, HMAC. Digital signatures and Authentication protocols: Digital signatures, Authentication Protocols, Digital signature standards. 36 2013-14

Authentication Applications: Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT–VI

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management. Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction. Intruders, Viruses and Worms, Intruders, Viruses and Related threats.

Fire Walls: Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. William Stallings, "*Cryptography and Network Security: Principles and Practice*",Pearson Education.
2. William Stallings,*"Network Security Essentials (Applications and Standards)",* Pearson Education.

REFERENCES:

1. Eric Maiwald, "*Fundamentals of Network Security*", Dreamtech press.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "*Network Security - Private Communication in a Public World*", PHI.
3. Whitman,*"Principles of Information Security",* Thomson.
4. Robert Bragg, Mark Rhodes, "*Network Security: The complete reference*", TMH
5. Buchmann, "*Introduction to Cryptography*".

I M.Tech I SEMESTER (ELECTIVE-II)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MEC1TH05	**IMAGE AND VIDEO PROCESSING**						

COURSE OBJECTIVES:

- This course offers fundamentals of digital image and video processing and algorithms for most of the work currently underway in this field.
- The students will get a clear impression of the breadth and practical scope of digital image and video processing
- To develop conceptual understanding which will enable them to undertake further study, research and/or implementation work in this area.

COURSE OUTCOME:

At the end of the course the students will be able to:

CO1: Describe the fundamentals of image and video processing and their applications
CO2: Develop familiarity and implement basic image and video processing algorithms.
CO3: Select and apply appropriate technique to real problems in image and video analysis.

UNIT –I

Fundamentals of Image Processing: Image Transforms: Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing Introduction, Need for transform, image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms**.**

UNIT –II

Image Enhancement: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters. Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering. Image Restoration: Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution.

UNIT –III

Image Segmentation: Introduction to image segmentation, Point, Line and Edge Detection, Region based segmentation., Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform.

UNIT-IV

Image Compression: Introduction, Need for image compression, Redundancy in images, Classification of redundancy in images, image compression scheme, Classification of image compression schemes, Fundamentals of information theory, Run length coding, Shannon – Fano coding, Huffman coding, Arithmetic coding, Predictive coding, Transformed based compression, Image compression standard, Wavelet-based image compression, JPEG Standards.

UNIT -V Basic Steps of Video Processing:

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT –VI

2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.
2. Video Processing and Communication – Yao Wang, JoemOstermann and Ya–quin Zhang. 1st Ed., PH Int.
3. S.Jayaraman, S.Esakkirajan and T.VeeraKumar, "Digital Image processing, Tata McGraw Hill publishers, 2009 REFRENCE BOOKS:
4. Digital Image Processing and Analysis-Human and Computer Vision Application with CVIP Tools – ScotteUmbaugh, 2nd Ed, CRC Press, 2011.
5. Digital Video Processing – M. Tekalp, Prentice Hall International. 9. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar – TMH, 2009.
6. Multidimentional Signal, Image and Video Processing and Coding – John Woods, 2nd Ed, Elsevier.
7. Digital Image Processing with MATLAB and Labview – Vipula Singh, Elsevier.
8. Video Demystified – A Hand Book for the Digital Engineer – Keith Jack, 5th Ed., Elsevier.

I M.Tech I SEMESTER (ELECTIVE-II)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS1TH12	**MOBILE COMPUTING TECHNOLOGIES**						

COURSE OBJECTIVES:

- Student will learn the basic concepts of mobile computing architecture, and cellular technologies like GSM, GPS, GPRS, CDMA and 3G.
- Student will impart the knowledge in WAP Clint programming, Palm OS and windows CE architecture.
- Student will comprehend the voice over internet protocol and security issue in the mobile computing.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Describe mobile computing and its applications and services.

CO2: Explain the concepts of cellular technologies like GSM. GPS, CDMA, GPRS AND 3G.

CO3: Comprehend the basics of wireless application protocol and fundamentals of intelligent networks.

CO4: Explain client programming windows CE architecture programming for GUI.

CO5: Describe the basics of voice over IP-H.23 frame work, real time protocols and IP multimedia systems.

CO6: Discuss the security techniques and algorithms and security framework environment

UNIT–I

Introduction to Mobile Computing Architecture: Mobile Computing – Dialog Control – Networks –Middleware and Gateways – Application and Services – Developing Mobile Computing Applications– Security in Mobile Computing – Architecture for Mobile Computing – Three Tier Architecture –Design considerations for Mobile Computing – Mobile Computing through Internet – Making existingApplications Mobile Enabled.

UNIT–II

Cellular Technologies: GSM, GPS, GPRS, CDMA and 3G: Bluetooth – RadioFrequencyIdentification – Wireless Broadband – Mobile IP – Internet Protocol Version 6 (IPv6) –Java Card – GSM Architecture – GSM Entities – Call Routing in GSM – PLMN Interfaces – GSMaddresses and Identifiers – Network aspects in GSM – Authentication and Security – Mobilecomputing over SMS – GPRS and Packet Data Network – GPRS Network Architecture – GPRSNetwork Operations – Data Services in GPRS – Applications for GPRS – Limitations of GPRS –Spread Spectrum technology – Is-95 – CDMA Versus GSM – Wireless Data – Third GenerationNetworks – Applications on 3G.

UNIT–III

Wireless Application Protocol (WAP) and Wireless LAN: WAP – MMS – WirelessLANAdvantages – IEEE 802.11 Standards – Wireless LAN Architecture – Mobility in wireless LAN.

Intelligent Networks and Interworking : Introduction – Fundamentals of Call processing – Intelligence in the Networks – SS#7 Signaling – IN Conceptual Model (INCM) – soft switch –Programmable Networks – Technologies and Interfaces for IN

UNIT–IV

Client Programming, Palm OS, Symbian OS, Win CE Architecture: Introduction – Movingbeyondthe Desktop – A Peek under the Hood: Hardware Overview – Mobile phones – PDA – DesignConstraints in Applications for Handheld Devices – Palm OS architecture – Application Development– Multimedia – Symbian OS Architecture – Applications for Symbian, Different flavors of WindowsCE -Windows CE Architecture.

J2ME: JAVA in the Handset – The Three-prong approach to JAVA Everywhere – JAVA 2MicroEdition (J2ME) technology – Programming for CLDC – GUI in MIDP – UI Design Issues –Multimedia– Record Management System – Communication in MIDP – Security considerations in MIDP –Optional Packages

UNIT–V

Voice Over Internet Protocol and Convergence: Voice over IP- H.323 Framework for Voice over IP– Session Initiation Protocol – Comparison between H.323 and SIP – Real Time protocols –Convergence Technologies – Call Routing – Voice over IP Applications – IP multimedia subsystem(IMS) – Mobile VoIP.

UNIT–VI

Security Issues in Mobile Computing: Introduction – Information Security – SecurityTechniquesand Algorithms – Security Protocols – Public Key Infrastructure – Trust – Security Models– Security frameworks for Mobile Environment.

TEXT BOOKS:

1.Asoke K Talukder,Roopa R Yavagal, "*Mobile Computing – Technology, Applications and Service Creation*", TATA McGraw Hill, 2009.

2. Jochen Schiller, "*Mobile Communications*", 2nd Edition, Pearson Education

REFERENCES:

1. VieriVaughi, Alexander DamnJaonvic,"*The CDMA 2000 System for Mobile Communications"*, Pearson.

2. Adalestein ,"*Fundamentals of Mobile &Parvasive Computing*", TMH, 2008.

I M.Tech I SEMESTER (ELECTIVE-II)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS1TH13	**ALGORITHMS FOR VLSI DESIGN AUTOMATION**						

COURSE OBJECTIVES:

- Explain the concepts of Physical Design Process such as partitioning, Floorplanning, Placement and Routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Simulation in VLSI Design Automation
- Formulate CAD design problems using algorithmic methods.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Place the blocks and how to partition the blocks while for designing the layout for IC.

CO2: Solve the performance issues in circuit layout.

CO3: Decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing

CO4: Analyze circuits using both analytical and CAD tools.

UNIT- I

Preliminaries: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT-II

General Purpose Methods For Combinational Optimization: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT- III

Layout Compaction, Placement, Floor Planning and Routing: Problems, Concepts and Algorithms**.**

Modeling and simulation: Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT -IV

Logic Synthesis And Verification: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.**High-Level Synthesis:** Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT- V

Physical Design Automation Of Fpgas: FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models. PHYSICAL DESIGN AUTOMATION OF MCMs : MCM technologies, MCM physical design cycle, Partitioning,

UNIT-VI

Placement: Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS:

1.S.H. Gerez, “Algorithms for VLSI Design Automation”, 1999, WILEY Student Edition, John Wiley & Sons (Asia) Pvt. Ltd.

2.Naveed Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, 2005, Springer International Edition.

REFERENCE BOOKS:

1.Hill & Peterson, “Computer Aided Logical Design with Emphasis on VLSI”, 1993, Wiley.

2.Wayne Wolf, “Modern VLSI Design: Systems on silicon”, 2nd ed., 1998, Pearson Education Asia.

I M.Tech I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	0	0	6	40	60	100	3
Code: 19MEC1LB01	**DESIGN AND SIMULATION LABORATORY**						

COURSE OBJECTIVES:

- Student able to design logic gates.
- Student able to learn about converters.
- Student able to explain the importance of embedded theory

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Design logic gates and ALU.
CO2: Design Finite State Machine logic Circuit.
CO3: Design Combinational circuits like Full Adder.
CO4: Design A to D & D to A converters.
CO5: Implement BANKER'S algorithm.

PART-A

VLSI Lab (Front-end Environment)

• The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/ Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/ FPGA kits).

• The students are required to acquire the knowledge in both the Platforms (Xilinx and Mentor graphics) by perform at least FOUR experiments on each Platform.

LIST OF EXPERIMENTS:

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter.
4. Synchronous RAM.
5. ALU.
6. UART Model.
7. Traffic Light Controller using Sequential Logic circuits
8. Finite State Machine (FSM) based logic circuit.

PART-B

VLSI Lab (Back-end Environment)

• The students are required to design and implement the Layout of the following experiments of any THREE using CMOS 130nm Technology with Mentor Graphics Tool. 38 2013-14

LIST OF EXPERIMENTS:

1. Inverter Characteristics.

2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Digital-to-Analog-Converter.
6. Analog-to-Digital Converter.

LAB REQUIREMENTS FOR PART-A AND PART-B:

Software: Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool.

Hardware: Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

PART-C

Embedded Systems Laboratory

• The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits.

• The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.

• The students are required to perform at least THREE experiments.

LIST OF EXPERIMENTS: (using ARM-926 with PERFECT RTOS)

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
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5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.

Lab Requirements for PART-C:

Software:

(i) Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOSLibrary

(ii) LINUX Environment for the compilation using Eclipse IDE & Java withlatest version.

Hardware:

(i) The development kits of ARM-926 Developer Kits Boards.

(ii) Serial Cables, Network Cables and recommended power supply for theboard.

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I M.Tech II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MEC2TH03	**CMOS ANALOG AND DIGITAL IC DESIGN**						

COURSE OBJECTIVES:

- Explain the behavior of MOS Devices and Small-Signal & Large-Signal Modelingof MOS Transistor and Analog Sub-Circuits.
- Comprehend the design concepts of Combinational and Sequential MOS logic circuits.
- Extend the concepts of Sub circuits and CMOS Amplifiers like Differential Amplifiers,
- Cascode Amplifiers, Output Amplifiers, and Operational Amplifiers.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Design MOS devices and estimate their Electrical behavior.
CO2: Design Combinational MOS logic circuits.
CO3: Design Sequential MOS logic circuits.
CO4: Use the Dynamic logic circuits and Memories.
CO5: Extend the Analog Circuit Design to Different Applications in Real Time.
CO6: Measure characteristics of CMOS amplifiers.

UNIT-I

MOS Devices and Modeling: The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large- Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

MOS Design: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III

Sequential MOS Logic Circuits: Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT -IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

UNIT -V

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT-VI

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

TEXT BOOKS:

1. Ken Martin, "*Digital Integrated Circuit Design*", Oxford University Press, 2011.
2. Sung-Mo Kang, Yusuf Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", 3rd Ed., TMH, 2011.
3.Philip E. Allen and Douglas R. Holberg, "*CMOS Analog Circuit Design*", Oxford University Press, International Second Edition/Indian Edition, 2010.
4. Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, "*Analysis and Design of Analog Integrated Circuits*",Fifth Edition, Wiley India, 2010.

REFERENCES:

1. David A. Johns, Ken Martin, "*Analog Integrated Circuit Design*", Wiley Student Edn, 2013.
2. BehzadRazavi, "*Design of Analog CMOS Integrated Circuits*", TMH Edition.
3. Baker, Li and Boyce, "*CMOS: Circuit Design, Layout and Simulation*", PHI.
4. Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, *"Digital Integrated Circuits – A Design Perspective"*, 2nd Ed., PHI.

I M.Tech II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MEC2TH02	**DSP PROCESSORS AND ARCHITECTURES**						

COURSE OBJECTIVES:

- Explain digital signal processing techniques, implementation of DSP & FFT &their computational accuracies in DSP implementation.
- Comprehend the concepts of DSP Processor and its architectures and program a DSP processor to filter signals.
- Extend the concepts of various DSP device families & Interfacing of P-DSPs with Memory and peripherals

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Comprehends the knowledge & concepts of digital signal processing techniques, basic building blocks, implementation of DSP & FFT algorithms
CO2: Estimate their computational accuracies in DSP implementation.
CO3: Design Programmable DSP devices
CO4: Use the DSP processors TMS 320C 54XX for implementation of DSP algorithms & its interfacing techniques with various I/O peripherals.
CO5: Use various Analog Device Family of DSP Devices
CO6: Interface Memory and I/O Peripherals to DSP processors.

UNIT–I

Introduction to Digital Signal Processing: Introduction, A Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT–II

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT–III

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT-IV

Programmable Digital Signal Processors: Commercial Digital signal processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of MS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts ofTMS320C54XX processors, Pipeline operation of TMS320C54XX Processors.

UNIT–V

Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Blackfin Processor - The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of HardwareProcessing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT -VI

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan, "*Digital Signal Processing*", Thomson Publications, 2004.
2. K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, *"A Practical Approach to Digital Signal Processing"*, New Age International, 2006/2009
3. Woon-SengGan, Sen M. Kuo, "*Embedded Signal Processing with the Micro Signal Architecture Publisher*", Wiley-IEEE Press, 2007

REFERENCES:

1.B. Venkataramani and M. Bhaskar, *"Digital Signal Processors, Architecture, Programming and Applications ",* TMH, 2002.
2. Jonatham Stein, "*Digital Signal Processing*", John Wiley, 2005.
3. Lapsley et al.,"*DSP Processor Fundamentals, Architectures & Features*", S. Chand & Co.,2000.
4. *Digital Signal Processing Applications Using the ADSP-2100 Family,* The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI.
5. Steven W. Smith, "*The Scientist and Engineer's Guide to Digital Signal Processing*", California Technical Publishing, ISBN 0- 9660176-3-3, 1997
6. David J. Katz and Rick Gentile,"*Embedded Media Processing*", Analog Devices, Newnes , ISBN 0750679123, 2005.

I M.Tech II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH04	**EMBEDDED SYSTEM DESIGN**						

COURSE OBJECTIVES:

- To introduce students to the modern embedded systems and
- To show how to write programs for systems using a concrete platform built around.

COURSE OUTCOMES:

After studying this course students are able to

CO1: Describe the differences between the general computing system and the embedded system, also recognize the classification of embedded systems.

CO2: Becomes aware of interrupts, hyper threading and software optimization.

CO3: Design real time embedded systems using the concepts of RTOS.

CO4: Analyze various examples of embedded systems based on ATOM processor.

UNIT-I

Introduction : An Embedded System-Definition, Examples, Current Technologies, Integration in system Design, Embedded system design flow, hardware design concepts, software development, processor in an embedded system and other hardware units, introduction to processor based embedded system design concepts.

UNIT-II

Embedded Hardware : Embedded hardware building blocks, Embedded Processors – ISA architecture models, Internal processor design, processor performance, Board Memory – ROM, RAM, Auxiliary Memory, Memory Management of External Memory, Board Memory and performance. Embedded board Input / output – Serial versus Parallel I/O, interfacing the I/O components, I/O components and performance, Board buses – Bus arbitration and timing, Integrating the Bus with other board components, Bus performance.

UNIT-III

Embedded Software : Device drivers, Device Drivers for interrupt-Handling, Memory device drivers, On-board bus device drivers, Board I/O drivers, Explanation about above drivers with suitable examples.Embedded operating systems – Multitasking and process Management, Memory Management, I/O and file system management, OS standards example – POSIX, OS performance guidelines, Board support packages, Middleware and Application Software – Middle ware, Middleware examples, Application layer software examples.

UNIT-IV

Embedded System Design and Development: Embedded system design and development lifecycle model, creating an embedded system architecture, introduction to embedded software development process and tools- Host and Target machines, linking and locating software, Getting embedded software into the target system, issues in Hardware-Software design and co-design.

UNIT-V

Embedded System Implementation and Testing: Implementing the design-The main software utility tool, CAD and the hardware, Translation tools, Debugging tools, testing on host machine, simulators, Laboratory tools, System Boot-Up.

UNIT-VI

Embedded System Design-Case Studies Case studies:Processor design approach of an embedded system –Power PC Processor based and Micro Blaze Processor based Embedded system design on Xilinx platform-NiosII Processor based Embedded system design on Altera platform-Respective Processor architectures should be taken into consideration while designing an Embedded System.

TEXT BOOKS:

1. Tammy Noergaard "Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers", Elsevier(Singapore) Pvt.Ltd.Publications, 2005.
2. Frank Vahid, Tony D. Givargis, "Embedded system Design: A Unified Hardware/Software Introduction", John Wily & Sons Inc.2002.

REFERENCE BOOKS:

1. Peter Marwedel, "Embedded System Design", Science Publishers, 2007.
2. Arnold S Burger, "Embedded System Design", CMP.
3. Rajkamal, "Embedded Systems: Architecture, Programming and Design", TMH Publications, Second Edition, 2008.

I M.Tech II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH05	**ADHOC AND WIRELESS SENSOR NETWORKS**						

COURSE OBJECTIVES:

- Students will be able to describe the unique issues in IEEE 802.11 standard, Bluetooth Adhoc /sensor networks.
- Students will be able to discuss the challenges in designing mac, routing and transport protocols for wireless ad-hoc/sensor networks.
- Students will be able to comprehend the challenges in quality of service energy management, usage of mac protocols for sensor networks.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Demonstrate the LANs and PANs, mobile IP and optimizing web over wireless.

CO2: Explain the concepts of Ad Hoc wireless networks and their applications.

CO3: Comprehend the basics of routing protocol, classification and its application to Ad Hoc wireless network.

CO4: Discuss the transport and security protocols, their applications to Ad Hoc WSN and their challenges.

CO5: Discuss the issue and challenges of quality of service and energy management IN Ad hoc WSN.

CO6: Explain the basic concepts of WSN, data gathering and their issues.

UNIT-I

Wireless LANS and PANS: Introduction, Fundamentals of WLANS, IEEE 802.11Standard,HIPERLAN Standard, Bluetooth, Home RF.

Wireless Internet: Wireless Internet, Mobile IP, TCP in Wireless Domain, WAP, Optimizing Web over Wireless.

UNIT-II

AD HOC Wireless Networks: Introduction, Issues in Ad Hoc Wireless Networks, Ad Hoc Wireless Internet.

MAC Protocols for Ad Hoc Wireless Networks: Introduction, Issues in Designing a MACprotocolfor Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc WirelessNetworks, Classifications of MAC Protocols, Contention - Based Protocols, Contention – BasedProtocols with reservation Mechanisms, Contention – Based MAC Protocols with SchedulingMechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT –III

Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols,

On –Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT–IV

Transport Layer and Security Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks, Security in Ad Hoc Wireless Networks, Network Security Requirements, Issues and Challenges in Security Provisioning, Network Security Attacks, Key Management, Secure Routing in Ad Hoc Wireless Networks.

UNIT–V

Quality of Service: Introduction, Issues and Challenges in Providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions, MAC Layer Solutions, Network Layer Solutions, QoS Frameworks for Ad Hoc Wireless Networks.

Energy Management: Introduction, Need for Energy Management in Ad Hoc Wireless Networks, Classification of Ad Hoc Wireless Networks, Battery Management Schemes, Transmission Power Management Schemes, System Power Management Schemes.

UNIT–VI

Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

TEXT BOOKS:

1. C. Siva Ram Murthy and B.S.Manoj, "*Ad Hoc Wireless Networks: Architectures and Protocols*", PHI, 2004.
2. JagannathanSarangapani, "*Wireless Ad- hoc and Sensor Networks: Protocols, Performanceand Control*", CRC Press.

REFERENCES:

1.C.K. Toh, "*Ad-Hoc Mobile Wireless Networks: Protocols & Systems*", Pearson Education.
2. C. S. Raghavendra, Krishna M. Sivalingam, "Wireless Sensor Networks", Springer, 2004.

I M.Tech II SEMESTER (ELECTIVE-III)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH06	**SYSTEM ON CHIP DESIGN**						

COURSE OBJECTIVES:

- Students will be introduce to system architectural concepts and complexities, concepts of processors
- Students will be able to explain the fundamentals of memory design for SoC and inter connections.
- Students will be able to perform the mapping, reconfiguration design approaches and image compression.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Explain the system architectural concepts
CO2: Discuss the concepts processor micro architecture instructional handling.
CO3: Extend the SoC memory concepts and models of simple processor memory instructions
CO4: Discuss the interconnection concepts and SoCcustomization.
CO5: Comprehend the applications of SoC ,AES algorithms and image compression

UNIT-I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT-III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV

Interconnect Customization: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor.

UNIT-V

Interconnect Configuration: Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT-VI

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, "*Computer System Design System-on-Chip*", Wiely India Pvt. Ltd.
2. Steve Furber,"*ARM System on Chip Architecture*", 2nd Ed., Addison Wesley Professional, 2000.

REFERENCES:

1. Ricardo Reis, "*Design of System on a Chip: Devices and Components*", 1st Ed., Springer, 2004
2. Jason Andrews,"*Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)*" — Newnes, BK and CDROM.
3. PrakashRashinkar, Peter Paterson and Leena Singh L, "*System on Chip Verification – Methodologies and Techniques*", 2001, Kluwer Academic Publishers.

I M.Tech II SEMESTER (ELECTIVE-III)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH07	**SOFT COMPUTING TECHNIQUES**						

COURSE OBJECTIVES:

- To comprehend the architecture of intelligent control and concepts of artificial neural networks.
- To have an exposure about basic concepts of and its control methodologies of fuzzy logic system.
- To know the basic concepts of genetic algorithm, its steps, GA applications and fuzzy logic controller using MATLAB.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Describe the intelligent control architecture and rule based systems.
CO2: Realize the concepts of artificial neural network sand basic mathematical.
CO3: Demonstrate fuzzy logic system, basic operation and approximate reasoning..
CO4: Explain the fuzzy logic modeling and control schemes.
CO5: Comprehend the basic concepts of Genetic algorithms and its detailed steps. .
CO6: Extend the applications of genetic algorithm.

UNIT–I

Introduction: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT–II

Artificial Neural Networks: Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT–III

Fuzzy Logic System: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inference and defuzzification, Fuzzy knowledge and rule bases

UNIT– IV

Fuzzy Logic Control: Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT–V

Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and ant-colony search techniques for solving optimization problems.

UNIT –VI

Applications: GA application to power system optimization problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS:

1. Jacek.M.Zurada, "*Introduction to Artificial Neural Systems*", Jaico Publishing House, 1999.
2. Kosko, B,"*Neural Networks and Fuzzy Systems*", Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCES:

1.Klir G.J. and Folger T.A.,"*Fuzzy Sets, Uncertainty and Information*", Prentice-Hall of India Pvt. Ltd., 1993.
2. Zimmerman H.J.,"*Fuzzy Set Theory and Its Applications*", Kluwer Academic Publishers, 1994.
3. Driankov, Hellendroon, "Introduction *to Fuzzy Control*", Narosa Publishers.
4. Dr. B. Yagananarayana, "*Artificial Neural Networks*", PHI, New Delhi, 1999.
5. KishanMehrotra, Chelkuri K. Mohan, Sanjay Ranka, "*Elements of Artificial Neural Networks*", Penram International.
6. Simon Haykin, "*Artificial Neural Network*", 2nd Ed., Pearson Education.
7. S.N. Shivanandam, S. Sumati, S. N. Deepa, "*Introduction Neural Networks Using MATLAB 6.0*", 1/e, TMH, New Delhi.

I M.Tech II SEMESTER (ELECTIVE-III)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH08	**CYBER SECURITY**						

COURSE OBJECTIVES:

- To demonstrate about cyber crimes and how they are planned
- To expalin the vulnerabilities of mobile and wireless devices

COUESE OUTCOMES:

By end of this course, the students will able to

CO1: Evaluate the computer network and information security needs of an organization.
CO2: Assess cyber security risk management policies in order to adequately protect an organization's critical information and assets.
CO3: Measure the performance of security systems within an enterprise-level information system.
CO4: Troubleshoot, maintain and update an enterprise-level information security system.
CO5: Implement continuous network monitoring and provide real-time security solutions.
CO6: Formulate, update and communicate short- and long-term organizational cyber security strategies and policies.

UNIT- I

Introduction to Cybercrime: Introduction, Cybercrime, and Information security, who are cyber criminals, Classifications of Cybercrimes, Cybercrime: The legal Perspectives and Indian Perspective, Cybercrime and the Indian ITA 2000, A Global Perspective on Cybercrimes. Cyber offenses: How criminals Plan Them: Introduction, How Criminals plan the Attacks, Social Engineering, Cyber stalking, Cyber cafe and Cybercrimes, Botnets: The Fuel for Cybercrime, Attack Vector, Cloud Computing.

UNIT- II

Cybercrime: Mobile and Wireless Devices: Introduction, Proliferation of Mobile and Wireless Devices, Trends in Mobility, Credit card Frauds in Mobile and Wireless Computing Era, Security Challenges Posed by Mobile Devices, Registry Settings for Mobile Devices, Authentication service Security, Attacks on Mobile/Cell Phones,

Mobile Devices: Security Implications for Organizations, Organizational Measures for Handling Mobile, Organizational Security Policies an Measures in Mobile Computing Era, Laptops.

UNIT – III

Cybercrimes: Introduction, Cyber Crime and Legal Landscape around the world, Why Do We Need Cyber laws: The Indian Context, The Indian IT Act, Challenges to Indian Law and Cybercrime Scenario In India,

UNIT – IV

Cyber security: Digital signatures and the Indian IT Act, Amendments to the Indian IT Act, Cybercrime and Punishment Cyber law, Technology and Students: Indian Scenario.

UNIT – V

Understanding Computer Forensics: Introduction, Historical background of Cyber forensics, Digital Forensics Science, The Need for Computer Forensics, Cyber Forensics and Digital evidence, Forensics Analysis of Email, Digital Forensics Lifecycle, Chain of Custody concept, Network Forensics, Approaching a computer, Forensics Investigation, Challenges in Computer Forensics, Special Tools and Techniques Forensics Auditing

UNIT – VI

Organizational Implications: Introduction, Cost of Cybercrimes and IPR issues, Web threats for Organizations, Security and Privacy Implications, Social media marketing: Security Risks and Perils for Organizations, Social Computing and the associated challenges for Organizations.

TEXT BOOK:

1. Cyber Security: Understanding Cyber Crimes, Computer Forensics and Legal Perspectives, Nina Godbole and Sunil Belapure, Wiley INDIA.
2. Introduction to Cyber Security , Chwan-Hwa(john) Wu,J.David Irwin.CRC Press T&F Group

REFERENCE BOOK:

1. Cyber Security Essentials, James Graham, Richard Howard and Ryan Otson, CRC Press.

I M.Tech II SEMESTER (ELECTIVE-III)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH09	**ADVANCED DIGITAL SYSTEM DESIGN**						

COURSE OBJECTIVES:

The student will be able to

- Analyze of Synchronous and Asynchronous Sequential circuits.
- Introduced to Multi-Input system control design.
- To Implement the System Controllers using Combinational and Sequential Circuits.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Analyze Procedural Design steps of Synchronous.
CO2: Analyze Procedural Design steps of Asynchronous Sequential circuits.
CO3: Design Synchronous and Asynchronous Sequential circuits.
CO4: Apply Multi-Input system control design concepts to develop Different Vending Machine applications in Real Time.
CO5: Design System Controllers using Combinational MSI/LSI Circuits.
CO6: Design Programmable System Controllers using Sequential Circuits.

UNIT-I

Synchronous Sequential Circuit Design: Analysis of clocked synchronous sequential circuits – Moore / Mealy State diagrams, State Table, State Reduction and Assignment - Design of synchronous sequential circuits.

UNIT-II

Analysis Of Asynchronous Sequential Circuit : Analysis of asynchronous sequential circuit – Cycles – Races - Static, Dynamic and Essential hazards – Primitive Flow Table.

UNIT-III

Asynchronous Sequential Circuit Design: State Reductions and State Assignment - Design of asynchronous sequential circuits.

UNIT-IV

VEM and Introduction to Multi-Input System Controller Design: Variable Entered Maps – simplification - System Controllers – Design Phases – MDS DiagramGeneration – MDSD Symbology – Choosing the controller architecture – State Assignment – Next State decoder – Examples of 2s complement system and Pop Vending Machine – Concepts related to the use of conditional outputs.

UNIT-V

System Controllers Using Combinational MSI / LSI Circuits : Decoders and Multiplexers in system controllers – Indirect-Addressed MUX configuration – System controllers using ROM.

UNIT-VI

Sequential and Programmable System Controllers : System controllers using Shift Registers and Counters – General requirements of a programmable controller - Microinstructions – Programmable controllers with fixed instruction set.

TEXT BOOKS:

1.William I. Fletcher,"*An Engineering Approach to Digital Design*", Prentice Hall India, 2011

2.Charles H.RothJr, "*Fundamentals of Logic Design*", Thomson Learning,2004

REFERENCES:

1.Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001

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I I M.Tech II SEMESTER (ELECTIVE-III)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MEC2TH01	**CODING THEORY AND APPLICATIONS**						

COURSE OBJECTIVES:

- Student able to differentiate the types of errors and error detection.
- Student able to compute and detect errors in cyclic and convolutional codes.
- Student able to compute Syndrome and iterative algorithms and error correcting codes.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Measure average and entropy.
CO2: Implement Design hamming code.
CO3: Compute cyclic hamming codes and shortened cyclic codes.
CO4: Compute conventional codes like encoding of conventional codes.
CO5: Decode single burst error correcting cyclic codes.
CO6: Compute iterative algorithms.

UNIT –I

Coding for Reliable Digital Transmission and Storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

UNIT–II

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT–III

Cyclic Codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT–IV

Convolutional Codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT–V

Burst –Error-Correcting Codes: Decoding of Single-Burst error Correcting Cyclic codes, Single-Burst-Error-Correcting Cyclic codes, Burst-Error-Correcting Convolutional Codes, Bounds on Burst Error- Correcting Capability, Interleaved Cyclic and Convolutional Codes, Phased-Burst –Error-Correcting Cyclic and Convolutional codes.

UNIT -VI

BCH – Codes: BCH code- Definition, Minimum distance and BCH Bounds, Decoding Procedure for BCH Codes- Syndrome Computation and Iterative Algorithms, Error Location Polynomials and Numbers for single and double error correction

TEXT BOOKS:

1. Shu Lin, Daniel J.Costello,Jr, "*Error Control Coding- Fundamentals and Applications*", Prentice Hall, Inc.
2. Man Young Rhee, "Error *Correcting Coding Theory*", McGraw-Hill Publishing, 1989.

REFERENCES:

1. Bernard Sklar, "*Digital Communications-Fundamental and Application*",PE.
2. John G. Proakis, "*Digital Communications*", 5th Ed., TMH, 2008.
3. Salvatore Gravano,"*Introduction to Error Control Codes*", Oxford.
4. Todd K.Moon, "*Error Correction Coding – Mathematical Methods and Algorithms*", Wiley India, 2006.
5. Ranjan Bose, "*Information Theory, Coding and Cryptography*", 2nd Ed., TMH, 2009.

I M.Tech II SEMESTER (ELECTIVE-IV)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH10	**EMBEDDED REAL TIME OPERATING SYSTEMS**						

COURSE OBJECTIVES:

- Describe what makes a system a real -time system
- Explaisn the presence of and describe the characteristics of latency in real-time systems.
- Summarize special concerns that real -time systems present and how these concerns are addressed.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Design embedded systems and real-time systems for real time systems.

CO2: Identify the general structure and unique characteristics of real -time systems

CO3: Evaluate the need for real-time operating system. Implement the real-time operating system principles

CO4: Define the unique design problems and challenges of real-time systems

CO5: Apply real-time systems design techniques to various software programs.

CO6: Program an embedded system. Design, implement and test an embedded system.

UNIT-I

Introduction OS Services, Process Management, Timer Functions, Event Functions, Memory Management, Device, File and IO Systems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls.

UNIT-II

Real-Time Operating Systems: Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latencyand Response of the Tasks as Performance Metrics, OS Security Issues.

UNIT-III

RTOS Programming Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS-II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS OSEK, RTOS Linux 2.6.x and RTOS RT Linux.

UNIT-IV

Program Modeling – Case Studies Case study of embedded system design and coding for an Automatic Chocolate Vending Machine (ACVM) Using Mucos RTOS, case study of digital camera hardware and software architecture, case study of coding for sending application layer byte streams on a TCP/IP Network Using RTOS Vx Works, CaseStudy of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of

Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs.

UNIT-V

Target Image Creation & Programming in Linux Off-The-Shelf Operating Systems, Operating System Software, Target Image Creation for Window XP Embedded, Porting RTOS on a Micro Controller based Development Board. Overview and programming concepts of Unix/Linux Programming, Shell Programming, System Programming.

UNIT-VI

Programming in RT Linux Overview of RT Linux, Core RT Linux API, Program to display a message periodically, semaphore management, Mutex, Management, Case Study of Appliance Control by RT Linux System.

TEXT BOOKS:

1. Dr. K.V.K.K. Prasad: "*Embedded/Real-Time Systems*" Dream Tech Publications, Black pad book.
2. Rajkamal: "*Embedded Systems-Architecture*, *Programming and Design*", Tata McGraw Hill Publications, Second Edition, 2008.

REFERENCE BOOKS:

1. Labrosse, "*Embedding system building blocks* ", CMP publishers.
2. Rob Williams," *Real time Systems Development*", Butterworth Heinemann Publications.

I M.Tech II SEMESTER (ELECTIVE-IV)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH11	**HIGH SPEED NETWORKS**						

COURSE OBJECTIVES:

- Learns about high speed networks
- To facilitates the students on the basis of ATM and Frame relay concepts and explain the various types of LANs and to know about their applications.
- Enable the students to know techniques involved to support real-time traffic and congestion control in ATM.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Describe the ISDN and B-ISDN architecture and protocols.
CO2: Describe the ATM service categories, ATM cell header, ATM adaptation layer
CO3: Describe the various networks and routing algorithms
CO4: Understand of computer and networked system organization and architecture and knowledge of recent advances, current practices and trends in computer systems.
CO5: Comprehend TCP/IP networks management
CO6: Describe high speed networks.

UNIT-I

Network Services and Layered Architecture: Traffic characterization and quality of service, Network services, High performance networks, Network elements, Basic network mechanisms, layered architecture.

UNIT-II

ISDN & B-ISDN: Over view of ISDN, ISDN channels, User access, ISDN protocols, Brief history of B-ISDN and ATM, ATM based services and applications, principles and building block of B-ISDN, general architecture of B-ISDN, frame relay.

UNIT-III

ATM NETWORKS: Network layering, switching of virtual channels and virtual paths, applications of virtual channels and connections. QOS parameters, traffic descriptors, ATM service categories, ATM cell header, ATM layer, ATM adaptation layer.

UNIT-IV

INTERCONNECTION NETWORKS: Introduction, Banyan Networks, Routing algorithm & blocking phenomenon, Batcher-Banyan networks, crossbar switch, three stage class networks. REARRANGEABLE NETWORKS: Rearrangeable class networks, folding algorithm, bens network, looping algorithm.

UNIT-V

ATM SIGNALING, ROUTING AND TRAFFIC CONTROL: ATM addressing, UNI signalling, PNNI signalling, PNNI routing, ABR Traffic management.

UNIT-VI

TCP/IP NETWORKS: History of TCP/IP, TCP application and Services, Motivation, TCP, UDP, IP services and Header formats, Internetworking, TCP congestion control, Queue **management:** Passive & active, QOSin IP networks: differentiated and integrated services.

TEXT BOOKS:

1. William Stallings, "*ISDN & B-ISDN with Frame Relay*", PHI.
2. Leon Garcia widjaja, "*Communication Networks*", TMH, 2000.

REFERENCES:

1. N. N. Biswas, "*ATM Fundamentals*", Adventure books publishers, 1998.

I M.Tech II SEMESTER (ELECTIVE-IV)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH13	**DATA COMMUNICATION AND NETWORKS**						

COURSE OBJECTIVES:

- Introduces computer networks and concentrates on building a firm foundation for understanding Data Communications and Computer Networks.
- It is based around the OSI Reference Model that deals with the major issues in the bottom three (Physical, Data Link and Network) layers of the model.
- Introduces routers, gateways and application services.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Explain OSI Reference Model and in particular have a good knowledge of Physical, Data Link and Network layers.

CO2: Analyze the requirements for a given organizational structure and select the most appropriate networking architecture and technologies.

CO3: Explain the data link layer and HDLC and MAC protocols.

CO4: Specify and identify deficiencies in existing protocols, and then go onto formulate new and better protocols.

CO5: Comprehend the routers and gateways.

CO6: Extend simple mail transfer, file transfer, hypertext transfer protocols and multimedia applications.

UNIT-I

Introduction : Components of network - Topologies - WAN / LAN - OSI - ISO layered Architecture - Modulation and demodulation - Bit error rates - Line coding - Error correcting codes.

UNIT-II

Data Link Layer: Design issues - CRC technique and sliding window techniques - Performance analysis of sliding window techniques - Framing formats - Case Study.

UNIT-III

HDLC protocols : Medium access control - CSMA / CD - Token ring and token bus - FDDI - Wireless LAN - Performance analysis of MAC protocols - Bridges.

Network Layer : Circuit switching - packet switching - Design issues - IP addressing and IP diagram.

UNIT-IV

Routers and Gateways : Routing -Sub netting - CIDR - ICMP - ARP - RARP - IPv6 - QoS.

UNIT-V

Transport Layer TCPAnd UDP: Error handling and flow control - Congestion control – TCP Retransmission - Timeout - Socket Abstraction.

UNIT-VI:

Application Services: Simple Mail Transfer Protocol (SMTP) - File Transfer Protocols (FTP), telnet, the World Wide Web (WWW). Hypertext Transfer Protocol (HTTP), Domain name service (DNS), Security, Multimedia applications.

TEXT BOOKS:

1. William Stallings, "*Data and Computer Communications*", Seventh Edition, Prentice Hall, 2003.
2. Larry Peterson, Bruce S Davie, "*Computer Networks: A Systems Approach*",2nd Edition, Morgan Kaufmann Publishers, 1999.

REFERENCES:

1. James F Kurose, "*Computer Networking: A Top - Down Approach Featuring the Internet*", 2nd Edition 2002, Addison Wesley.
2. W.Richard Stevens and Gary R Wright, "*TCP / IP Illustrated*", Addison Wesley, Volume 1

& 2, 2001.

I M.Tech II SEMESTER (ELECTIVE-IV)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH12	**ADVANCED DIGITAL COMMUNICATION**						

COURSE OBJECTIVES:

- To comprehend the digital passband transmission and different types of digital modulation techniques.
- To analyze the different channel coding techniques and design considerations of a digital communication system.
- To extend the concept of spread spectrum communication system.

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Analyze the performance of a pass band digital communication system in terms of error rate and spectral efficiency.
CO2: Analyze Performance of various digital modulation techniques.
CO3: Analyze Performance of various channel coding techniques.
CO4: Perform the time and frequency domain analysis of the signals in a digital communication system.
CO5: Select the blocks in a design of digital communication system.
CO6: Analyze Performance of spread spectrum communication system.

UNIT-I

Digital Passband Transmission: Introduction, Pass band Transmission Model, Gram-Schmidt Orthogonalization Procedure, Geometric Interpretation of Signals, Response of Bank of Correlators to Noisy Input, Coherent Detection of Signals in Noise, Probability of Error, Correlation Receiver, Detection of Signals with unknown Phase.

UNIT-II

Digital Modulation Techniques I: Hierarchy of Digital Modulation Techniques, Coherent Binary PSK, Coherent Binary FSK, Coherent Quadriphase-Shift Keying, Coherent Minimum Shift Keying, Noncoherent Orthogonal Modulation, Noncoherent Binary Frequency-Shift Keying.

UNIT-III

Digital Modulation Techniques II: Differential Phase-Shift Keying, Comparison of Binary and Quaternary Modulation Schemes, M-ary Modulation Techniques, Power Spectra, Band-width Efficiency, Synchronization.

UNIT-IV

Channel Coding : Introduction, Discrete Memory less Channels, Linear Block Codes, Cyclic Codes, Convolution Codes, Maximum Likelihood Decoding of Convolution codes, Trellis-Coded Modulation, Coding for Compounded-Error Channels.

UNIT-V

Design Considerations Of A Digital Communication System : Inter symbol Interference, Nyquist's Criterion for Distortion less Baseband Binary Transmission, Correlative-Level Coding, Error Probability Plane, Bandwidth Efficiency Plane, Modulation and coding tradeoffs, defining, designing, and evaluating digital communication system, Modulation and coding for band limited channels.

UNIT-VI

Spread Spectrum Techniques: Pseudo noise sequences, Direct sequence Spread Spectrum systems, Frequency hopping systems, Synchronization and Jamming Considerations.

TEXT BOOKS:

1. Simon Haykin, *"Digital communication"*, Third Edition, John Wiley and Sons.
(Units I, III & IV)
2. B.Sklar, *"Digital Communications"*, Second Edition, Pearson Education Asia.
(Units II & IV)

REFERENCES:

1. J.G. Proakis, "*Digital Communications*", Third Edition, McGraw Hill.

I M.Tech II SEMESTER (ELECTIVE-IV)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	0	0	40	60	100	3
Code: 19MDS2TH14	**EMBEDDED NETWORKING**						

COURSE OBJECTIVES:

- To learn embedded communication protocols and ISA/PCI parallel bus protocols and to learn
- USB and CAN bus protocols
- To learn basic of Ethernet and to learn the basics of embedded Ethernet
- To learn the basics of wireless embedded networking

COURSE OUTCOMES:

By end of this course, the students will able to

CO1: Explain different embedded communication protocol
CO2: Comprehend the basic concepts of Ethernet, USB and CAN
CO3: Explain embedded Ethernet message exchange process
CO4: Extend the embedded wireless embedded networking

UNIT–I

Embedded Communication Protocols: Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT–II

USB and CAN BUS: USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs.

UNIT–III

CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT–IV

Ethernet Basics: Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT–V

Embedded Ethernet: Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT–VI

Wireless Embedded Networking: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization – Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

TEXT BOOKS:

1. Frank Vahid, Tony Givargis, "*Embedded Systems Design: A Unified Hardware/Software Introduction*", John & Wiley Publications, 2002
2. Jan Axelson, "*Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port*",Penram Publications, 1996.

REFERENCES:

1. Dogan Ibrahim, "*Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18Fseries*", Elsevier 2008.
2. Jan Axelson, "*Embedded Ethernet and Internet Complete*",Penram publications, 2003.
3. BhaskarKrishnamachari ,"*Networking Wireless Sensors*", Cambridge press, 2005.

I M.Tech II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	0	0	6	40	60	100	3
Code: 19MDS2LB01	**EMBEDDED SYSTEMS LABORATORY**						

COURSE OBJECTIVES:

- Experimenting on ARM-926 with perfect RTOS
- Experimenting on ARM-CORTEX processor using any open source RTOS. (Coo-Cox-Software- Platform)

COURSE OUTCOMES:

By end of this course, the students will able to write programs on

- register a command, create a new task, interrupt handling
- allocate resource using semaphore, share resource using MUTEX
- avoid deadlock using Banker's algorithm, synchronize two identical threads using Monitor program and readers/writers problem for concurrent tasks
- implementation of interfacing of display with the ARM- CORTEX processor
- interface ADC and DAC ports with the Input and Output sensitive devices
- Simulate the temperature DATA Logger with the SERIAL communication with PC
- Implementation of developer board as a modem for data communication using serial port communication between two PCs

- The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits and ARM-Cortex.
- The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.
- The students are required to perform at least SIX experiments from Part-I and TWO experiments from Part-II.

LIST OF EXPERIMENTS:

Part-I : Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.

Part-II Experiments on ARM-CORTEX processor using any open source RTOS. (Coo-Cox-Software- Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.

2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication with PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PCs.

LAB REQUIREMENTS:

Software:

(i) Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.
(ii) LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

(i) The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.
(ii) Serial Cables, Network Cables and recommended power supply for the board.