Narasaraopeta Engineering College (Autonomous)

Kotappakonda Road, Yellamanda (P.O), Narasaraopet- 522601, Guntur District, AP.
Sponsored by Gayatri Educational Development Society, Narasaraopet.
Approved by AICTE, New Delhi & Permanently affiliated to JNTUK, Kakinada. Code: 47.
Twice Accredited by NBA & NAAC with "A" Grade; ISO 9001:2008 Certified Institution.
Phone: 08647239905 Website: www.nrtenggcollege.com Email: nrtec_principal@yahoo.com

DEPARTMENT OF ECE

M.TECH (DECS) ACADEMIC REGULATIONS

COURSE STRUCTURE & SYLLABUS

ACADEMIC REGULATIONS - 2019 FOR M.TECH

(Effective for the students admitted into I year from the Academic Year 2019-20 and onwards)

1. QUALIFICATION FOR ADMISSION

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit / rank obtained by the candidates at the qualifying entrance test GATE/PGECET or on the basis of any other order of merit as approved by the Government from time to time.

2. AWARD OF M.TECH. DEGREE

A student will be declared eligible for the award of the M. Tech. Degree, if he fulfils the following academic requirements.

(a) Pursue a course of study for not less than two academic years and not more than four academic years.

(b) The candidate registers for 80 credits and secure all 80 credits.

3. COURSES OF STUDY

The following courses of study are offered at present as specializations in the M.Tech. courses with English as medium of instruction.

S. No.	Specialization Code	Abbreviation
01	06 - DSCE	Digital Systems and Computer Electronics
02	15 - MD	Machine Design
03	21 - TE	Thermal Engineering
04	38 - DECS	Digital Electronics and Communication Systems
05	42 - P&ID	Power and Industrial Drives
06	58 - CSE	Computer Science and Engineering
07	87 - SE	Structural Engineering

And any other course as approved by the authorities from time to time.

4. STRUCTURE OF THE PROGRAMME

Semester	Credits
I M.TECH I SEM	21
I M.TECH II SEM	21
II M.TECH III SEM	38
II M.TECH IV SEM	
TOTAL	80

Each course is normally assigned a certain number of credits as follows:
- 3 credits for 4 lecture periods.
- 3 credits for 6 laboratory periods per week.
- 1 credit for seminar.
- 2 credits for comprehensive viva
- 35 credits for project work.

5. DISTRIBUTION AND WEIGHTAGE OF MARKS

The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks for theory / practical / seminar / comprehensive viva on the basis of internal evaluation and end semester examinations.

5.1 THEORY

All theory subjects consisting of 6 units in each subject, the assessment shall be for 40 marks through internal evaluation and 60 marks through external end semester examination of 3 hours duration.

5. 1.a. INTERNAL EVALUATION

The internal evaluation will be based on two cycle tests conducted in each semester. The 40 internal marks will be awarded as 75% of the best cycle and 25% of the least cycle examinations, where each cycle of examination contain
Descriptive test - 30 Marks
Assignment test - 10 Marks

Each descriptive test question paper contains3 questions one from each unit covering syllabus from 3 units (first 3 units for first cycle and the remaining 3 units for second cycle). The student has to answer all the three questions (3X10M=30M).The descriptive examination will be conducted for1½ hour duration.

In Assignment Tests 5 or 6 questions will be declared in the class room at least one week in advance. In the test, two questions (one from each unit) will be given at random to each student and the student has to answer it.
The Assignment Test-1 will be conducted for 10 marks covering the syllabus from 1st& 2ndunits.The Assignment Test-2 will be conducted for 10 marks from 4th& 5th units.

5.1.b. EXTERNAL EVALUATION

The question paper comprises of 8 questions, there should be one from each unit. Student has to answer 5 questions out of 8, each question carry 12marks (5X12=60). The duration of end theory examination is 3 hours.

5.2 PRACTICALS

For practical subjects evaluation is as follows during the semester

5.2.a. INTERNAL EVALUATION

There shall be continuous evaluation during the semester for 40 internal marks. The internal marks shall be awarded as follows:

Record	- 10 Marks
Day-to-day work	- 15 Marks
Internal Lab Test	- 15Marks

5.2.b. EXTERNAL EVALUATION

For practical subjects there shall be an external examination at the end of the semester for 60 marks in the presence of external examiner.

5.3 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the end semester examination and a minimum of 50% of the total marks in the end semester examination and internal evaluation taken together.

5.4 SEMINAR

For seminar, a student under the supervision of a faculty member shall collect the literature on an advanced topic related to his specialization and review the literature then submit it to the department in a report form during the third semester and shall make an oral presentation before the departmental review committee consisting of the supervisor and head of the department / a senior faculty member. There shall be an internal evaluation for 100 marks in the form of viva voce examination and assessment of report and its presentation. There will be NO external evaluation. A candidate shall be deemed to have secured the minimum academic requirement in seminar, if he secures a minimum of 50% of marks in the examination.

If a candidate fails to secure the minimum marks prescribed for successful completion, he has to re-register and he has to submit a fresh report and appear for the evaluation by the committee.

5.5 COMPREHENSIVE VIVA-VOCE

Comprehensive viva voce examination is conducted during the 3rd semester in all the subjects of first & second semesters of the course by a committee consisting of two senior faculty members of the department. There will be NO external evaluation.

A candidate shall be deemed to have secured the minimum academic requirement in seminar, if he secures a minimum of 50% of marks in the examination.

If a candidate fails to secure the minimum marks prescribed for successful completion, he has to re-register and undergo viva voce examination.

5.6 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.3) he has to re-appear for the end semester examination in that subject.
A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate is less than 50% and has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate's attendance in the re-register subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks in the previous attempt stand cancelled. For re-registration the candidates have to apply to the college by paying the requisite fee and get approval from the authorities before the beginning of the semester in which re-registration is required.

5.7 In case the candidate secures less than the required attendance in any re-registered subject(s), he shall not be permitted to write the End examination in that subject. He shall again re-register the subject when next offered.

5.8 Laboratory examinations must be conducted with two examiners, one of them being the laboratory class teacher or teacher of the respective college and the second examiner shall be appointed by the Principal from the panel of examiners submitted by the respective departments.

5.9 PROJECT WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

5.9.1. A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members.

5.9.2. Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

5.9.3. After satisfying 5.9.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work for approval. The students can initiate the Project work, only after obtaining the approval from the Project Review Committee (PRC).

5.9.4. If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Project Review Committee (PRC). However, the Project Review Committee (PRC) shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of supervisor or topic as the case may be.

5.9.5. A candidate shall submit his status report in two stages at least with a gap of 3 months between them.

5.9.6. The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical subjects with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical subjects before submission of the Thesis.

5.9.7. Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.

5.9.8. The thesis shall be adjudicated by one examiner selected by the authorities. For this, the HOD of the concerned dept. shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned.

5.9.9. If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is unfavourable again, the thesis shall be summarily rejected. The candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the authorities.

5.9.10. If the report of the examiner is favourable, viva-voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the thesis. The Board shall jointly report the candidate's work as one of the following: Grade O(Outstanding)/ Grade A(Excellent)/Grade B(Very Good) /Grade C(Good)/ Grade D(Pass)/ Grade F(Fail).

The Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination.

5.9.11. If the report of the viva-voce is Grade F, the candidate shall retake the viva-voce examination only after three months. If he fails to get a satisfactory report at the second viva-voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the authorities.

6. ATTENDANCE REQUIREMENTS:

(i) A student shall be eligible to appear for the end examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

(ii) Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester for genuine medical reasons and shall be approved by a

committee duly appointed by the college. A fee stipulated by the college shall be payable towards condonation of shortage of attendance. However the number of condonations is restricted to two for the entire course.

(iii) A student who is short of attendance in a semester may seek re-admission into that semester when offered next time, within 4 weeks from the date of commencement of class work.

(iv) If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for re-admission into the same class.

7. COURSE PATTERN:

(i) The entire course of study is of two academic years and every year will have TWO Semesters.

(ii) A student is eligible to appear for the end examination in a subject, but absent for it or has failed in the end examinations may appear for that subject in supplementary examinations, when conducted next.

(iii) When a student is detained due to shortage of attendance, he may be re-admitted in to the same semester/year in which he has been detained.

8. METHOD FOR AWARDING OF GRADE POINTS FOR A SUBJECT:

Theory/ Laboratory / Seminar/ Comprehensive viva/ Project (% of marks in a subject)	Corresponding Grade Points	Letter Grade
91 - 100	10	O (Outstanding)
81 - 90	9	A (Excellent)
71 - 80	8	B (Very Good)
61 - 70	7	C (Good)
51 - 60	6	D (Pass)
< 50	0	F (Fail)

9. Criteria for award of grades/division.

9.1 Calculation of Semester Grade Point Average (SGPA)* for semester

The performance of each student at the end of each semester is indicated in terms of SGPA. The SGPA is calculated as given below:

$$\text{SGPA} = \frac{\sum (CR \, X \, GP)}{\sum CR}$$

Where CR= Credits of a subject

GP = Grade Points awarded for a subject

*SGPA is calculated for a candidate who passed all the subjects in that semester.

9.2 Calculation of Cumulative Grade Point Average (CGPA) for Entire Program:

The CGPA is calculated as given below:

$$\text{CGPA} = \frac{\sum (CR \, X \, GP)}{\sum CR}$$

Where CR = Credits of a subject
GP = Grade Points awarded for a subject

- The SGPA and CGPA shall be rounded off to 2 decimal point and reported in the transcripts.
- Equivalent percentage = (CGPA – 0.75) x 10

9.3 Award of Division:

After satisfying the requirements prescribed for the completion of the program, the student shall be eligible for the award of M.Tech Degree and shall be placed in one of the following classes:

CGPA	Class
≥ 7.75	First Class with Distinction (Provided all the subjects should pass in the first attempt)
≥ 6.75	First Class (with subject failures)
≥ 5.75 & < 6.75	Second Class

10. REVALUATION:

1. Student can submit the application for revaluation, along with the prescribed fee for revaluation of his answer script(s) of theory subject(s) as per the notification issued by the Controller of Examinations.

2. The Controller of Examinations shall arrange for revaluation of such answer script(s).

3. An External examiner, other than the first examiner shall revaluate the answer script(s).

11. MINIMUM INSTRUCTION DAYS:

The minimum instruction days for each semester shall be 90 working days.

12. There shall be no branch transfer after the completion of admission process.

13. WITHHOLDING OF RESULTS

If the student has not paid the dues, if any, to the college or if any case of indiscipline is pending against him, the result of such student will be kept withheld. His degree will be withheld in such cases.

1.

14. TRANSITORY REGULATIONS

Discontinued or detained candidates are eligible for readmission as and when next offered.

A candidate, who is detained or discontinued in a semester, on readmission shall be required to do all the subjects in the curriculum prescribed for the batch of students in which the student joins subsequently. However, exemption will be given to those candidates who have already passed such subjects in the earlier semester(s) he was originally admitted into and substitute subjects are offered in place of them as decided by the Board of Studies. However, the decision of the Board of Studies will be final.

14.1 A student who is following JNTUK curriculum and detained due to shortage of attendance at the end of the first semester of first year shall join the autonomous batch of first year first semester. Such students shall study all the subjects prescribed for the batch in which the student joins and considered on par with regular candidates of Autonomous stream and will be governed by the autonomous regulations.

14.2 A student who is following JNTUK curriculum, detained due to shortage of attendance at the end of the second semester of first year or at the subsequent semesters shall join with the autonomous batch in the appropriate semester. Such candidates shall be required to pass in all the subjects in the program prescribed by the Board of Studies concerned for that batch of students from that semester onwards to be eligible for the award of degree. However, exemption will be given in the subjects of the semester(s) of the batch which he had passed earlier and substitute subjects will be offered in place of them as decided by the Board of Studies. The student has to clear all his backlog subjects up to previous semester by appearing for the supplementary examinations conducted by JNTUK for the award of degree will be sum of the credits up to previous semester under JNTUK regulations and the credits prescribed for the semester in which a candidate seeks readmission and subsequent semesters under the autonomous stream. The class will be awarded based on the academic performance of a student in the autonomous pattern.

****

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT INEXAMINATIONS

- The Principal shall refer the cases of Malpractices in Internal Assessment Test and Semester end examinations to a malpractice prevention committee constituted by him for the purpose. Such committee shall follow the approved levels of punishment. The Principal shall take necessary action against the students based on the recommendations of the committee.

- Any action by the candidate trying to get undue advantage in the performance or trying to help another, or derive the same through unfair means is punishable according to the provisions contained hereunder:

	Nature of Malpractices/ Improper conduct	**Punishment**
	If the candidate:	
1(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination).	Expulsion from the examination hall and cancellation of the performance in that subject only.
1(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination(theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the college.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall.

		The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from classwork and all college examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from classwork and all college examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent /any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-incharge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words,	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s)has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will

	either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from classwork and all college examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6to 8.	Student of the college expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also

		debarred and forfeits the seat. Person(s) who do not belong to the college will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the college for further action to award suitable punishment.	

OTHER MATTERS:

1. Physically challenged candidates who have availed additional examination time and a scribe during their UG / PGECET examinations will be given similar concessions on production of relevant proof / documents.

2. The Principal shall deal in an appropriate manner with any academic problem which is not covered under these rules and regulations, in consultation with the Heads of the departments and subsequently such actions shall be placed before the Academic Council for ratification. Any emergency modification of regulation, approved in the meetings of the Heads of the departments shall be reported to the Academic Council for ratification.

GENERAL:

1. The academic council may, from time to time, revise, amend or change the regulations, schemes of examinations and / or syllabi.
2. Wherever the words ‘’he’’ ‘’him’’ ‘’his’’, occur in the regulations, they include ‘’she’’, ’’her’’, ’’hers’’.
3. The academic regulation should be read as a whole for the purpose of any interpretation.
4. In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the principal is final.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.TECH COURSE STRUCTURE
DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS (DECS)

I M.TECH-I SEMESTER

S.No.	Name of Subject	L	T	P	Internal Marks	External Marks	Total Marks	Credits
1	Digital System Design	4	-	-	40	60	100	3
2	Embedded Real Time Operating Systems	4	-	-	40	60	100	3
3	VLSI Technology and Design	4	-	-	40	60	100	3
4	Optical Communication Technology	4	-	-	40	60	100	3
5	**Elective I** i. Digital data communications ii. Adhoc Networks iii. System modeling and simulation iv. Design for IoT v. Image and Video Processing	4	-	-	40	60	100	3
6	**Elective II** i. Wireless communication and networks ii. Digital design using HDL iii. Radar Signal Processing iv. Adaptive Signal Processing v. Soft computing techniques	4	-	-	40	60	100	3
7	**Laboratory** Design and Simulation Laboratory	-	-	6	40	60	100	3
	TOTAL	**24**	**-**	**6**	**280**	**420**	**700**	**21**

I M.TECH-II SEMESTER

S.No.	Name of Subject	L	T	P	Internal Marks	External Marks	Total Marks	Credits
1	Coding Theory and Applications	4	-	-	40	60	100	3
2	Detection and Estimation Theory	4	-	-	40	60	100	3
3	DSP Processors and Architectures	4	-	-	40	60	100	3
4	Advanced Computer Architecture	4	-	-	40	60	100	3
5	**Elective III** i. CMOS Analog and Digital IC Design ii. Advanced Digital Signal Processing iii. RF Circuit Design iv. Embedded C v. Advanced mobile communication	4	-	-	40	60	100	3
6	**Elective IV** i. VLSI design automation ii. Nano technology iii. Advanced digital communication iv. Antennas for wireless Communication v. Advanced Microprocessors and Microcontrollers	4	-	-	40	60	100	3
7	**Laboratory** Advanced Communications Laboratory	-	-	6	40	60	100	3
	TOTAL	**24**	**-**	**6**	**280**	**420**	**700**	**21**

II M.TECH-III & IV SEMESTERS

S.No.	Name of Subject	Total Marks	Credits
1	Seminar	100	1
2	Comprehensive Viva-Voce	100	2
3	Project	-	35
	TOTAL	200	**38**

I M.TECH-I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE1TH01				**DIGITAL SYSTEM DESIGN**			

Course Objectives:

- An ability to implement minimization of switching functions in different methods and implementation of CAMP Algorithm.
- An ability to synthesize logic and state machines using a PLA design and minimization and implementation of state machines using Field-Programmable Gate Arrays, CPLDs etc.
- An ability to design a computer to be fault-tolerant for combinational circuits and sequential circuits.

Course Outcomes:

By the end of the course, the student will be able to

- Perform minimization of switching functions in different methods.
- Implement CAMP Algorithm.
- Synthesize logic and state machines using a PLA design and minimization
- Design state machines using Field-Programmable Gate Arrays.
- Construct a computer to be fault-tolerant for combinational circuits.
- Design a computer to be fault-tolerant for sequential circuits.

UNIT-I

Introduction to Minimization Procedures:

Review on minimization of switching functions using tabular methods, K-map, QM algorithm,

UNIT-II

CAMP Algorithm:

CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-III

PLA Design, Minimization and Folding Algorithms:

Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm (IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT -IV

Design of Large Scale Digital Systems:

Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, and PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-V

Fault Diagnosis in Combinational Circuits:

Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built-in-self-test.

UNIT-VI

Fault Diagnosis in Sequential Circuits:

Fault detection and location in sequential circuits, circuit test approach, initial state identification, Hamming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS:

1. N. N. Biswas, "*Logic Design Theory*", PHI.
2. Z. Kohavi, "*Switching and Finite Automata Theory*", 2nd Edition, TMH, 2001.
3. Parag K. Lala, "*Digital System Design using PLDs*", PHI, 1984.

REFERENCES:

1. Charles H. Roth, "*Fundamentals of Logic Design*", 5th Ed., Cengage Learning.
2. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, "*Digital Systems Testing and Testable Design*", John Wiley & Sons Inc.

I M.TECH-I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE1TH08				**EMBEDDED REAL TIME OPERATING SYSTEMS**			

Course Objectives:

- Describe what makes a system a real -time system
- Explain the presence of and describe the characteristics of latency in real-time systems.
- Summarize special concerns that real -time systems present and how these concerns are addressed.

Course Outcomes:

By the end of the course, the student will be able to

- Design embedded systems and real-time systems For real time systems.
- Identify the general structure and unique characteristics of real -time systems
- Evaluate the need for real-time operating system. Implement the real-time operating system principles
- Define the unique design problems and challenges of real-time systems
- Apply real-time systems design techniques to various software programs.
- Program an embedded system. Design, implement and test an embedded system. Ex: real time + embedded : games on a Game boy or arcade games Ex: real time: Spore on a laptop

UNIT-I

Introduction: OS Services, Process Management, Timer Functions, Event Functions, Memory Management, Device, File and IO Systems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls.

UNIT-II

Real-Time Operating System: Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latency and Response of the Tasks as Performance Metrics, OS Security Issues.

UNIT-III

RTOS Programming: Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS-II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS OSEK, RTOS Linux 2.6.x and RTOS RT Linux.

UNIT-IV

Program Modeling – Case Studies: Case study of embedded system design and coding for an Automatic Chocolate Vending Machine (ACVM) Using Mucos RTOS, case study of digital camera hardware and software architecture, case study of coding for sending application layer byte streams on a TCP/IP Network Using RTOS Vx Works, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs.

UNIT-V

Target Image Creation & Programming in Linux: Off-The-Shelf Operating Systems, Operating System Software, Target Image Creation for Window XP Embedded, Porting RTOS on a Micro Controller based Development Board. Overview and programming concepts of Unix/Linux Programming, Shell Programming, System Programming.

UNIT-VI

Programming in RT Linux: Overview of RT Linux, Core RT Linux API, Program to display a message periodically, semaphore management, Mutex, Management, Case Study of Appliance Control by RT Linux System.

TEXT BOOKS:

1. Dr. K.V.K.K. Prasad, "*Embedded/Real-Time Systems*", Dream Tech Publications.
2. Rajkamal, "*Embedded Systems-Architecture, Programming and Design*", Second Edition, Tata McGraw Hill Publications, 2008.

REFERENCES:

1. Labrosse, "*Embedding system building blocks* ", CMP publishers.
2. Rob Williams," *Real time Systems Development*", Butterworth Heinemann Publications.

I M.TECH-I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MEC1TH02				**VLSI TECHNOLOGY AND DESIGN**			

Course Objectives:

- To examine the basic building blocks of large-scale digital integrated circuit.
- To introduce about Planar technology, electrical properties of MOS, CMOS and BiCMOS circuits.
- To familiarize with VLSI design steps and chip design methodologies.

Course Outcomes:

By the end of the course, the student will be able to

- Identify IC fabrication technology and various electrical properties of MOS, CMOS and BiCMOS circuits..
- Design various logic circuits using MOS and CMOS transistors..
- Analyze chip design methods.
- Synthesize digital circuits using VHDL.
- Design logic circuit layouts for both static CMOS
- Compute the power consumption of a VLSI chip.

UNIT-I

VLSI Technology: Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.
VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT-II

CMOS VLSI Design: MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies**,** comparison of different processes.
Building Blocks of a VLSI circuit: Computer architecture, memory architectures, communication interfaces, mixed signal interfaces.

UNIT-III

VLSI Design Issues: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

UNIT-IV

Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitative and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT-V

Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.

Subsystem Design Processes: Some general considerations and an illustration of design processes, design of an ALU subsystem.

UNIT-VI

Floor Planning: Introduction**,** Floor planning methods, off-chip connections.

Architecture Design: Introduction, Register-Transfer design, high level synthesis, architectures for low power, architecture testing.

Chip Design: Introduction and design methodologies.

TEXT BOOKS:

1. K. Eshraghian, Douglas A. Pucknell, Sholeh Eshraghian, "*Essentials of VLSI Circuits and Systems"*, PHI Publications, 2005.
2. Wayne Wolf, *"Modern VLSI Design"*, 3rd Ed., Pearson Education, 1997.
3. Dr.K.V.K.K.Prasad, KattulaShyamala, *"VLSI Design"*, Kogent Learning Solutions Inc., 2012.

REFERENCES:

1. Randall L.Geiger, Phillip E.Allen, Noel R.Strader, *"VLSI Design Technologies for Analog and Digital Circuits"*, TMH Publications, 2010.
2. Ming-BO Lin, *"Introduction to VLSI Systems: A Logic, Circuit and System Perspective"*, CRC Press, 2011.
3. N.H.E Weste, K. Eshraghian, "*Principals of CMOS VLSI Design*", 2nd Edition, Addison Wesley.

I M.TECH-I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE1TH09				**OPTICAL COMMUNICATION TECHNOLOGY**			

Course Objectives:

- To familiarize the basic elements of optical fiber transmission link, fiber modes configurations and structures.
- To examine the various optical source materials, LED structures, quantum efficiency,
  Laser diodes.
- To analyze the fiber optical network components, variety of networking aspects, FDDI, SONET/SDH and operational principles WDM.

Course Outcomes:

By the end of the course, the student will be able to

- Design a complete optical fiber communication system, to enable the design of data transmission optical systems.
- Demonstrate optical fiber propagation characteristics and transmission properties.
- Demonstrate light sources including the principles of laser action in semiconductors.
- The characteristics of optical transmitters based on semiconductor and external modulation techniques, and the characteristics of optical amplifiers.
- Describe the principles of photo detection and optical receiver sensitivity to the extent of the material presented.
- Demonstrate of fiber devices and multiple wavelength division multiplexing techniques to the extent of the material presented

UNIT–I

Signal propagation in Optical Fibers: Geometrical Optics approach and Wave Theory approach, Loss and Bandwidth, Chromatic Dispersion, Non Linear effects-Stimulated Brillouin and Stimulated Raman Scattering, Propagation in a Non-Linear Medium, Self- Phase Modulation and Cross Phase Modulation, Four Wave Mixing, Principle of Solitons.

UNIT–II

Fiber Optic Components for Communication & Networking: Couplers, Isolators and Circulators, Multiplexers, Bragg Gratings, Fabry-Perot Filters, Mach Zender Interferometers, Arrayed Waveguide Grating, Tunable Filters, High Channel Count Multiplexer Architectures, Optical Amplifiers, Direct and External Modulation Transmitters, Pump Sources for Amplifiers, Optical Switches and Wavelength Converters.

UNIT–III

Modulation: Signal formats for Modulation, Subcarrier Modulation and

Multiplexing, Optical Modulations – Duo binary, Single Side Band and Multilevel Schemes

UNIT-IV

Demodulation: Ideal and Practical receivers for Demodulation, Bit Error Rates, Timing Recovery and Equalization, Reed-Solomon Codes for Error Detection and Correction.

UNIT-V

Transmission System Engineering: System Model, Power Penalty in Transmitter and Receiver, Optical Amplifiers, Crosstalk and Reduction of Crosstalk, Cascaded Filters, Dispersion Limitations and Compensation Techniques.

UNIT–VI

Fiber Non-linearities and System Design Considerations: Limitation in High Speed and WDM Systems due to Non-linearities in Fibers, Wavelength Stabilization against Temperature Variations, Overall System Design considerations – Fiber Dispersion, Modulation, Non-Linear Effects, Wavelengths, All Optical Networks.

TEXT BOOKS:

1. Rajiv Ramaswami and Kumar N. Sivarajan, "*Optical Networks: A Practical Perspective*", 2nd Ed., 2004, Elsevier Morgan Kaufmann Publishers (An Imprint of Elsevier).
2. Gerd Keiser, "*Optical Fiber Communications*", 3rd Ed., McGraw Hill, 2000.

REFERENCES:

1. John. M. Senior, "*Optical Fiber Communications: Principles and Practice*", 2nd Ed., PEI, 2000.
2. Harold Kolimbris, "*Fiber Optics Communication*", 2nd Ed., PEI, 2004.
3. Uyless Black, "*Optical Networks: Third Generation Transport Systems*", 2nd Ed., PEI, 2009
4. Govind Agarwal, "*Optical Fiber Communications* ", 2nd Ed., TMH, 2004.
5. S.C. Gupta, "*Optical Fiber Communications and Its Applications*, PHI, 2004.

I M.TECH-I SEMESTER **(ELECTIVE-I)**	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MEC1TH03				**DIGITAL DATA COMMUNICATIONS**			

Course Objectives:

- Introduce students to the evolution of digital modulation schemes and the concepts data communication.
- Awareness of different error correction codes, data link protocols.
- Introduction of different networks and multiple access techniques.

Course Outcomes:

By the end of the course, the student will be able to

- Examine the different digital modulation schemes.
- Familiarize the different concepts of data communication.
- Analyze the different error correction codes.
- Develop the different data link protocols.
- Design the different networks and multiple access techniques.

UNIT -I

Digital Modulation Schemes:

BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

UNIT -II

Basic Concepts of Data Communications, Interfaces and Modems:

Data Communication Networks, Protocols and Standards, UART, USB, I2C, I2S, Line Configuration, Topology, Transmission Modes, Digital Data Transmission, DTE-DCE interface, Categories of Networks – TCP/ IP Protocol suite and Comparison with OSI model.

UNIT -III

Error Correction: Types of Errors, Vertical Redundancy Check (VRC), LRC, CRC, Checksum, Error Correction using Hamming code

UNIT -IV

Data Link Control: Line Discipline, Flow Control, Error Control

Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocols, Bit-Oriented Protocol, Link Access Procedures.

UNIT -V

Multiplexing: Frequency Division Multiplexing (FDM), Time Division Multiplexing (TDM), Multiplexing Application, DSL.

Local Area Networks: Ethernet, Other Ether Networks, Token Bus, Token Ring, FDDI.

Metropolitan Area Networks: IEEE 802.6, SMDS

Switching: Circuit Switching, Packet Switching, Message Switching.

Networking and Interfacing Devices: Repeaters, Bridges, Routers, Gateway, Other Devices.

UNIT -VI

Multiple Access Techniques:

Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization, Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA), Code Division Multiple Access (CDMA), OFDM and OFDMA.

TEXT BOOKS:

1. B. A.Forouzan, "*Data Communication and Computer Networking* ", 2nd Ed., TMH, 2003.
2. W. Tomasi, "*Advanced Electronic Communication Systems*", 5th Ed., PEI, 2008.

REFERENCES:

1. Prakash C. Gupta, "*Data Communications and Computer Networks*", PHI, 2006.
2. William Stallings, "*Data and Computer Communications*", 8th Ed., PHI, 2007.
3. T. Housely, "*Data Communication and Tele Processing Systems*", 2nd Ed., BSP, 2008.
4. Brijendra Singh, "*Data Communications and Computer Networks*", 2nd Ed., PHI, 2005.

I M.TECH-I SEMESTER **(ELECTIVE-I)**	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE1TH10				**ADHOC NETWORKS**			

Course Objectives:

- To examine the state-of-the-art in network protocols, architectures and applications.
- Analyze existing network protocols and networks.
- Develop new protocols in networking

Course Outcomes:

By the end of the course, the student will be able to

- Describe the unique issues in ad-hoc/sensor networks.
- Describe current technology trends for the implementation and deployment of wireless Adhoc/sensor networks.
- Discuss the challenges in designing MAC, routing and transport protocols for wireless Adhoc/sensor networks.
- Discuss the challenges in designing routing and transport protocols for wireless Adhoc/sensor networks.
- Comprehend the various sensor network Platforms, tools and applications.
- Design and develop the different network sensors and applications

UNIT-I

Introduction: Introduction of ad-hoc/sensor networks, Key definitions of adhoc/sensor networks - Advantages of ad-hoc/sensor networks - Unique constraints and challenges Driving Applications. Electromagnetic spectrum-Radio propagation mechanism characteristics of the wireless channel Adhoc Wireless Networks – Heterogeneity in Mobile Devices – Wireless Sensor Networks – Traffic Profiles – Types of Adhoc Mobile Communications – Types of Mobile Host Movements – Challenges Facing Adhoc Mobile Networks – Adhoc Wireless Internet.

UNIT-II

End To End Delivery And Security: Transport layer: Issues in designing- Transport layer classification, adhoc transport Protocols, Security issues in adhoc networks: issues and challenges, network security attacks, secure routing protocols AdHoc wireless networks Introductions to local area networks, wide area networks, MAN, PAN architectures and applications.

UNIT-III

Media Access Control (MAC) Protocols: Media Access Control (MAC) Protocols Introduction- Issues in Designing a MAC Protocol for Ad Hoc Wireless Networks – Classifications of MAC Protocol. MACAW – FAMA – BTMA – DPRMA – Real-Time MAC protocol – Multichannel Protocols – Power Aware MAC.

UNIT-IV

Routing Protocols: Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks – Classifications of Routing Protocols -Table-driven protocols – DSDV – WRP – CGSR – On- Demand protocols – DSR – AODV – TORA – LAR – ABR – Zone Routing Protocol – Power Aware Routing protocols.

UNIT-V

Networking Sensors And Applications: Unique features, Deployment of ad-hoc/sensor network –Sensor tasking and control Transport layer and security protocols.

UNIT-VI

Sensor Network Platforms And Tools: Berkley Motes - Sensor network programming challenges - Embedded Operating System – Simulators, Applications: Applications of Ad- Hoc/Sensor Network and Future Directions. Ultra wide band radio communication-Wireless fidelity systems.

TEXT BOOKS:

1. Karl, Holger, and Andreas Willig. "*Protocols and architectures for wireless sensor networks*", John Wiley & Sons, 2007.
2. C. Siva Ram Murthy and B. S. Manoj, "*Ad Hoc Wireless Networks: Architectures and Protocols*", Prentice Hall, 2004.

REFERENCES:

1. Feng Zhao and Leonidas J. Guibas, "*Wireless Sensor Networks: An Information Processing Approach*" Morgan Kaufmann, 2004.
2. Stefano Basagni, Marco Conti, Silvia Giordano and Ivan Stojmenovic, "*Mobile ad hoc Networking*", Wiley-IEEE press, 2004.
3. Mohammad Ilyas, "*The Handbook of Adhoc Wireless Networks*", CRC Press, 2002.

I M.TECH-I SEMESTER **(ELECTIVE-I)**	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MEC1TH04				**SYSTEM MODELING AND SIMULATION**			

Course Objectives:

- Students will study the system models, simulators.
- Students must be able to familiarize probability concepts in simulation and queuing theory.
- Students analyze about discrete system simulation, GPSS and SEMSCRIPT.

Course Outcomes:

By the end of the course, the student will be able to

- Describe, system models.
- Describe, simulators.
- Rapidly design probability concepts in simulation.
- Rapidly design queuing theory.
- Evaluate discrete system simulation.
- Analyze GPSS and SEMSCRIPT.

UNIT-I

System Models: Concepts, continuous and Discrete Systems, systems modeling, types of models, subsystems, corporate model, system study.
System simulation: Techniques, comparison of simulation and analytical methods, types of simulation, distributed log models, cobwed models.

UNIT-II

Continuous system simulation: Numerical solution of differential equations, analog computers, hybrid computers, continuous system simulation languages – CSMP, system dynamic growth models, logistic curves.

UNIT-III

Probability concepts in simulation: Monte Carlo techniques, stochastic variables, probability functions, random number generation algorithms.

UNIT-IV

Queuing Theory: Arrival pattern distribution, service times, queuing disciplines, measure of queues, mathematical solutions to queuing problems.

UNIT-V

Discrete Systems Simulation: Events generation of arrival patterns,simulation programming tasks, analysis of simulation output.

UNIT- VI

GPSS and SEMSCRIPT: General description of GPSS and SEMSCRIPT, programming in

GPSS.

Simulation Programming techniques: Data Structures, implementation of activities, events and queues, event scanning, simulation algorithms in GPSS and SEMSCRIPT.

TEXT BOOKS:

1. GeofferyGordan, *"Systems Simulation"*, PHI, 1978.

I M.TECH-I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
(ELECTIVE-I)	4	-	-	40	60	100	3
CODE: 19MDE1TH11				**DESIGN FOR IoT**			

Course Objectives:

- Students will be explored to the interconnection and integration of the physical world and the cyberspace.
- They are also able to design & develop IOT Devices.

Course Outcomes:

By the end of the course, the student will be able to

- Familiarize the application areas of IOT
- Realize the revolution of Internet in Mobile Devices, Cloud & Sensor Networks
- Design building blocks of Internet of Things and characteristics.

UNIT-I

Introduction & Concepts: Introduction to Internet of Things, Physical Design of IOT, Logical Design of IOT, IOT Enabling Technologies, IOT Levels.

UNIT-II

Domain Specific IOTs: Home Automation, Cities, Environment, Energy, Retail, Logistics, Agriculture, Industry, Health & Life Style.

UNIT-III

M2M & System Management with NETCONF-YANG: M2M, Difference between IOT and M2M, SDN and NFV for IOT, Software-defined Networking, Network Function Virtualization, Need for IOT Systems Management, Simple Network Management Protocol, Limitations of SNMP, Network Operator Requirements, NETCONF, YANG, IOT Systems management with NETCONF-YANG.

UNIT-IV

Developing Internet of Things & Logical Design using Python: Introduction, IOT Design Methodology, Installing Python, Python Data Types & Data Structures, Control Flow, Functions, Modules, Packages, File Handling, Date/ Time Operations, Classes, Python Packages

UNIT-V

IOT Physical Devices & Endpoints: What is an IOT Device, Exemplary Device, Board. Linux on Raspberry Pi, Interfaces, Programming & IOT Devices,

UNIT-VI

Case study & IoT Applications: IoT applications in home, infrastructure, buildings, security, industries, home appliances, other IoT electronic equipments. Sensors interfacing using Raspberry Pi, Arduino.

TEXT BOOKS:

1. Vijay Madisetti, ArshdeepBahga," Internet of Things A Hands-On- Approach",2014, ISBN:978 0996025515

REFERENCE BOOKS:

1. Adrian McEwen, "Designing the Internet of Things", Wiley Publishers, 2013, ISBN: 978-1-118-43062-0 2. Daniel Kellmereit, "The Silent Intelligence: The Internet of Things". 2013, ISBN

I M.TECH-I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
(ELECTIVE-I)	4	-	-	40	60	100	3
CODE:19MEC1TH05				**IMAGE AND VIDEO PROCESSING**			

Course Objectives:

- Student able to familiarize about fundamentals of image processing and image enhancement.
- Student able to gain knowledge about image segmentation and image compression
- Student able to analyze fundamentals about video processing and able to estimate multi -resolution motion.

Course Outcomes:

By the end of the course, the student will be able to

- Design Fourier transform and two-dimensional Fourier transform.
- Differentiate image restoration techniques.
- Differentiate segmentation techniques.
- Interpret importance of JPEG.
- Differentiate analog video and digital video.
- Estimate pixels in video

UNIT–I

Fundamentals of Image Processing and Image Transforms:

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing Introduction, Need for transform, image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform

Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

UNIT –II

Image Enhancement: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

Image Restoration: Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution.

UNIT–III

Image Segmentation: Introduction to image segmentation, Point, Line and Edge Detection, Region based segmentation. Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge Based segmentation, Edge detection and linking, Hough transform, Active contour

UNIT-IV

Image Compression: Introduction, Need for image compression, Redundancy in images, Classification of redundancy in images, image compression scheme, Classification of image compression schemes, Fundamentals of information theory, Run length coding, Shannon– Fano coding, Huffman coding, Arithmetic coding, Predictive coding, Transformed based compression, Image compression standard, Wavelet-based image compression, JPEG Standards.

UNIT-V

Basic Steps of Video Processing: Analog Video, Digital Video. Time- Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT–VI

2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Gonzaleze and Woods, "*Digital Image Processing*", 3rd Ed., Pearson.
2. Yao Wang, Joem Ostermann and Ya–quin Zhang, "*Video Processing and Communication*", 1st Ed., PH Int.
3. S. Jayaraman, S. Esakkirajan and T. VeeraKumar, "*Digital Image Processing*, Tata McGraw Hill publishers, 2009.

REFRENCES:

1. Scotte Umbaugh, "*Digital Image Processing and Analysis-Human and Computer Vision Application with CVIP Tools*", 2nd Ed, CRC Press, 2011.
2. M. Tekalp, "*Digital Video Processing* ", Prentice Hall International.
3. John Woods, "*Multidimentional Signal, Image and Video Processing and Coding*", 2nd Ed, Elsevier.
4. Vipula Singh, "*Digital Image Processing with MATLAB and Labview*", Elsevier.
5. Keith Jack, "*Video Demystified – A Hand Book for the Digital Engineer*", 5th Ed., Elsevier.

I M.TECH-I SEMESTER (ELECTIVE-II)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MEC1TH06				**WIRELESS COMMUNICATIONS AND NETWORKS**			

Course Objectives:

- To familiarize the concepts of basic cellular system, frequency reuse, channel assignment strategies, handoff strategies, interference.
- To Develop the Mobile radio propagation for small scale fading and multipath, large scale path loss.
- To discuss the different generations of mobile networks, WAN and IEEE 802.11.

Course Outcomes:

By the end of the course, the student will be able to

- Summarize the concepts of spectrum allocation, basic cellular system, frequency reuse, channel assignment strategies, handoff strategies, interference, improving coverage and capacity, cell splitting.
- Analyze the Mobile radio propagation large scale path loss.
- Develop the different outdoor propagation models.
- Design Mobile radio propagation for small scale fading and multipath.
- Evaluate the different equalizers and diversity techniques.
- Discuss the different wireless networks, development of wireless networks.

UNIT-I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity,

Channel planning for Wireless Systems, Adjacent Channel interference, Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring.

UNIT–II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction- Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering.

UNIT–III

Outdoor Propagation Models: Longley- Ryce Model, Okumura Model, Hata Model, PCS Extension to HataModel, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site

Specific Modeling.

UNIT–IV

Mobile Radio Propagation: Small –Scale Fading and Multipath Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel-Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT -V

Equalization and Diversity Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non-linear Equalization-Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Techniques- Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT -VI

Wireless Networks Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE
802.11 Medium Access Control, Comparison of IEEE 802.11 a, b, g and n standards, IEEE 802.16and its enhancements, Wireless PANs, Hiper Lan, WLL.

TEXT BOOKS:

1. Theodore, S. Rappaport, "*Wireless Communications, Principles, Practice*", 2nd Ed., PHI, 2002.
2. Andrea Goldsmith, "*Wireless Communications*", Cambridge University Press, 2005.
3. Gottapu Sasibhushana Rao, "*Mobile Cellular Communication*", Pearson Education, 2012.

REFERENCES:

1. Kaveh Pah Laven and P. Krishna Murthy, "*Principles of Wireless Networks*", PE, 2002.
2. Kamilo Feher, "*Wireless Digital Communications* ", PHI, 1999.
3. William Stallings, "*Wireless Communication and Networking*", PHI, 2003.
4. Upen Dalal, "*Wireless Communication*", Oxford Univ. Press.
5. Vijay K. Gary, "*Wireless Communications and Networking*", Elsevier.

I M.TECH-I SEMESTER **(ELECTIVE–II)**	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MEC1TH07				**DIGITAL DESIGN USING HDL**			

Course Objectives:

- Students will study the signals, variables, combinational logic circuit design using VHDL.
- Students must be able to design sequential logic circuit design using VHDL and digital logic circuits using Verilog HDL.
- Students discuss about synthesis and testing of digital logic circuit, CAD tools.

Course Outcomes:

By the end of the course, the student will be able to

- Demonstrate the use and application of signals, variables.
- Demonstrate the use and application of combinational logic circuit design using VHDL.
- Simulate and debug sequential logic circuit described in VHDL.
- Simulate and debug digital logic circuits using Verilog HDL.
- Synthesize digital circuits at several level of abstractions.
- Test digital logic using CAD tools

UNIT-I

Digital Logic Design using VHDL Introduction, designing with VHDL, design entry methods, logic synthesis , entities , architecture , packages and configurations, types of models: dataflow , behavioral , structural, signals vs. variables, generics, data types, concurrent vs. sequential statements , loops and program controls.

Digital Logic Design using Verilog HDL Introduction, Verilog Data types and Operators, Binary data manipulation, Combinational and Sequential logic design, Structural Models of Combinational Logic, Logic Simulation, Design Verification and Test Methodology, Propagation Delay, Truth Table models using Verilog.

UNIT-II

Combinational Logic Circuit Design using VHDL Combinational circuits building blocks: Multiplexers, Decoders , Encoders , Code converters, Arithmetic comparison circuits , VHDL for combinational circuits , Adders-Half Adder, Full Adder, Ripple-Carry Adder, Carry Look- Ahead Adder, Subtraction, Multiplication.

UNIT-III

Sequential Logic Circuit Design using VHDL Flip-flops, registers & counters, synchronous sequential circuits: Basic design steps, Mealy State model, Design of FSM using CAD tools, Serial Adder Example, State Minimization, Design of Counter using sequential Circuit approach.

UNIT-IV

Digital Logic Circuit Design Examples using Verilog HDL Behavioral modeling , Data types, Boolean-Equation-Based behavioral models of combinational logics ,

Propagation delay and continuous assignments, latches and level-sensitive circuits in Verilog, Cyclic behavioral models of flip-flops and latches and Edge detection, comparison of styles for behavioral model; Behavioral model, Multiplexers, Encoders and Digital Systems & Computer Electronics 33Decoders, Counters, Shift Registers, Register files, Dataflow models of a linear feedback shift register, Machines with multi cycle operations, ASM and ASMD charts for behavioral modeling, Design examples, Keypad scanner and encoder.

UNIT-V

Synthesis of Digital Logic Circuit Design Introduction to Synthesis, Synthesis of combinational logic, Synthesis of sequential logic with latches and flip-flops, Synthesis of Explicit and Implicit State Machines, Registers and counters.

UNIT-VI

Testing of Digital Logic Circuits and CAD Tools Testing of logic circuits, fault model, complexity of a test set, path-sensitization, circuits with tree structure, random tests, testing of sequential circuits, built in self test, printed circuit boards, computer aided design tools, synthesis, physical design.

TEXT BOOKS:

1. Stephen Brown &ZvonkoVranesic, "*Fundamentals of Digital logic design with VHDL*", Tata McGraw Hill,2nd edition.
2. Michael D. Ciletti, "*Advanced digital design with the Verilog HDL*", Eastern economy edition, PHI.

REFERENCES:

1. Stephen Brown & ZvonkoVranesic, "*Fundamentals of Digital logic with Verilog design*", Tata McGraw Hill,2nd edition.
2. Bhaskar, "*VHDL Primer*", 3rd Edition, PHI Publications.
3. Ian Grout, "*Digital systems design with FPGAs and CPLDs*", Elsevier Publications.

I M.TECH-I SEMESTER **(ELECTIVE-II)**	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE1TH12				**RADAR SIGNAL PROCESSING**			

Course Objectives:

- To provide operation of radar systems.
- To know different signal processing techniques.
- To provide pulse compression and coding techniques.

Course Outcomes:

By the end of the course, the student will be able to

- Describe operation of radar systems and discuss their main design parameters and components.
- Describe signals and waveforms used in radar systems.
- Discuss problems and design challenges in radar signaling and waveforms.
- Use various tools (or simulators) for signal and system level simulations in radar systems
- Discuss various signal processing techniques for various radar operations including MTI, pulse Doppler and SAR radars.
- Use various pulse Coding Techniques.

UNIT-I

Introduction: Radar Block Diagram, Radar Equation, Information Available from Radar Echo. Review of Radar Range Performance– General Radar Range Equation, Radar Detection with Noise Jamming, Beacon and Repeater Equations, Bistatic Radar.

UNIT-II

Matched Filter Receiver

Impulse Response, Frequency Response Characteristic and its Derivation, Matched Filter and Correlation Function, Correlation Detection and Cross-Correlation Receiver, Efficiency of Non-Matched Filters, Matched Filter for Non-White Noise.

UNIT-III

Detection of Radar Signals in Noise: Detection Criteria – Neyman-Pearson Observer, Likelihood-RatioReceiver, Inverse Probability Receiver, Sequential Observer, Detectors – Envelope Detector, Logarithmic Detector, I/Q Detector. Automatic Detection - CFAR Receiver, Cell Averaging CFAR Receiver, CFAR Loss, CFAR Uses in Radar. Radar Signal Management – Schematics, Component Parts, Resources and Constraints.

UNIT-IV

Waveform Selection: Radar Ambiguity Function and Ambiguity Diagram – Principles and Properties; Specific Cases – Ideal Case, Single Pulse of Sine Wave, Periodic Pulse Train, Single Linear FM Pulse, Noise Like Waveforms, Waveform Design Requirements, Optimum Waveforms for Detection in Clutter, Family of Radar Waveforms.

UNIT –V

Pulse Compression in Radar Signals: Introduction, Significance, Types, Linear FM Pulse Compression –Block Diagram, Characteristics, Reduction of Time Side lobes, Stretch Techniques, Generation and Decoding of FM Waveforms – Block Schematic and Characteristics of Passive System, Digital Compression, SAW Pulse Compression.

UNIT-VI

Phase Coding Techniques: Principles, Binary Phase Coding, Barker Codes, Maximal Length Sequences (MLS/LRS/PN), Block Diagram of a Phase Coded CW Radar. Poly Phase Codes : Frank Codes, Costas Codes, Non-Linear FM Pulse Compression, Doppler Tolerant PC Waveforms – Short Pulse, Linear Period Modulation (LPM/HFM), Sidelobe Reduction for Phase Coded PC Signals.

TEXT BOOKS:

1. M.I. Skolnik, "*Radar Handbook*", 2nd Ed., McGraw Hill, 1991.
2. Fred E. Nathanson, "*Radar Design Principles: Signal Processing and the Environment*", 2nd Ed., PHI, 1999.
3. M.I. Skolnik, "*Introduction to Radar Systems*", 3rd Ed., TMH, 2001.

REFERENCES:

1. Peyton Z. Peebles, Jr., "*Radar Principles*", John Wiley, 2004.
2. R. Nitzberg, "*Radar Signal Processing and Adaptive Systems* ", Artech House, 1999.
3. F.E. Nathanson, "*Radar Design Principles*", 1st Ed., McGraw Hill, 1969.

I M.TECH-I SEMESTER **(ELECTIVE–II)**	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE1TH13				**ADAPTIVE SIGNAL PROCESSING**			

Course Objectives:

- To understand the basics of adaptive system.
- To make familiar with gradient search algorithms and functions.
- To introduce LMS & RLS algorithms.
- To be acquainted with random variables and Kalman filters.

Course Outcomes:

By the end of the course, the student will be able to

- Comprehend design criteria and modelling adaptive systems and theoretical performance evaluation.
- Design a linear adaptive processor.
- Apply mathematical models for error performance and stability.
- Apply adaptive modeling systems for real time applications.
- Design based on Kalman filtering and extended Kaman filtering.

UNIT – I

ADAPTIVE SYSTEMS: Characteristics, Areas of application, general properties, open and closed loop adaptation, applications of closed loop adaptation, Example of an Adaptive System, The Adaptive Linear Combiner: Description, Weight Vectors, Desired Response, Performance Function; Gradient and Minimum Mean-Square Error.

Approaches to the Development of Adaptive Filter Theory: Introduction to Filtering Smoothing and Prediction-Linear Optimum Filtering, Problem Statement, Principle of Orthogonality, Minimum–Mean-Squared Error, Wiener –Hopf Equations, Error Performance, Normal Equation.

UNIT – II

GRADIENT SEARCHING**:** Searching the Performance Surface – Methods and Ideas of Gradient Search Methods, Gradient Searching Algorithm and its Solution, Stability and Rate of Convergence, Learning Curves, Gradient Search by Newton‟s Method, Method of Steepest Descent, Comparison of Learning Curves.

UNIT-III

GRADIENT ESTIMATION: Gradient component estimation by derivative measurement, the performance penalty, derivative measurement and performance penalties with multiple weights, variance of the gradient estimate, effects on the weight vector solution.

UNIT-IV:

LMS & RLS ALGORITHMS: Overview, LMS Adaptation Algorithms, Stability and Performance Analysis of LMS Algorithms, LMS Gradient and Stochastic Algorithms, Convergence of LMS Algorithms, RLS algorithms.

UNIT-V

ADAPTIVE MODELING AND SYSTEM IDENTIFICATION: General description, adaptive modeling of multipath communication channel, adaptive modeling in geophysical exploration, adaptive modeling in FIR digital filter synthesis, general description of inverse modeling, some theoretical examples.

UNIT-VI:

KALMAN FILTERING THEORY: Introduction, Recursive Mean Square Estimation for Scalar Random Variables, Statement of Kalman Filtering Problem, Innovation Process. Estimation of State using the Innovation Process, Filtering, Initial Conditions, Summary of Kalman Filters, Variants of the Kalman Filtering, the Extend Kalman Filtering, Identification as a Kalman Filtering Problem.

TEXT BOOKS:

1. Bernand Widrow, Samuel D. Stearns, "*Adaptive Signal Processing*", Pearson Education, Asia, 2009.

2. Simon Haykins, "*Adaptive filter Theory*", PHI, 2003.

REFERENCES BOOKS:

1. Sophocles J. Orfamidis, "*Optimum Signal Processing – An Introduction*", 2/e, McGraw Hill, 1990.

2. Alexander, Thomas S. "*Adaptive signal processing: theory and applications",* Springer Science & Business Media, 2012.

3. TulayAdali, Simon Haykin, "*Adaptive Signal Processing – Next Generation Solutions*", Wiley Publications, 2012.

I M.TECH-I SEMESTER (ELECTIVE–II)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE1TH14				**SOFT COMPUTING TECHNIQUES**			

Course Objectives:

- To study the architecture of intelligent control and concepts of artificial neural networks.
- To have an exposure about basic concepts of and its control methodologies of fuzzy logic system.
- To know the basic concepts of genetic algorithm, its steps, GA applications and fuzzy logic controller using MATLAB.

Course Outcomes:

By the end of the course, the student will be able to

- Gain the knowledge of intelligent control architecture and rule based systems.
- Realize the concepts of artificial neural network sand basic mathematical.
- Discuss about fuzzy logic system, basic operation and approximate reasoning..
- Develop the fuzzy logic modeling and control schemes.
- Discuss about basic concepts of Genetic algorithms and its detailed steps.
- Design the applications of genetic algorithm.

UNIT–I

Introduction: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation
- Expert systems.

UNIT–II

Artificial Neural Networks: Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT–III

Fuzzy Logic System: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inference and defuzzification, Fuzzy knowledge and rule bases

UNIT– IV

Fuzzy Logic Control: Fuzzy modeling and control schemes for nonlinear systems, Self- organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT–V

Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and ant-colony search techniques for solving optimization problems.

UNIT –VI

Applications: GA application to power system optimization problem, Case studies: Identification and control of linear and nonlinear dynamic systems using MATLAB-Neural Network toolbox, Stability analysis of Neural-Network interconnection systems, Implementation of fuzzy logic controller using MATLAB fuzzy-logic toolbox, Stability analysis of fuzzy control systems.

TEXT BOOKS:

1. Jacek.M.Zurada, "*Introduction to Artificial Neural Systems*", Jaico Publishing House, 1999.
2. Kosko, B," *Neural Networks and Fuzzy Systems*", Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCES:

1. Klir G.J. and Folger T.A., "*Fuzzy Sets, Uncertainty and Information*", Prentice-Hall of India Pvt. Ltd., 1993.
2. Zimmerman H.J., "*Fuzzy Set Theory and Its Applications*", Kluwer Academic Publishers, 1994.
3. Driankov, Hellendroon, "Introduction *to Fuzzy Control*", Narosa Publishers.
4. Dr. B. Yagananarayana, "*Artificial Neural Networks*", PHI, New Delhi, 1999.
5. Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka, "*Elements of Artificial Neural Networks*", Penram International.
6. Simon Haykin, "*Artificial Neural Network* ", 2nd Ed., Pearson Education.
7. S.N. Shivanandam, S. Sumati, S. N. Deepa, "*Introduction Neural Networks Using MATLAB 6.0*", 1/e, TMH, New Delhi.

I M.TECH-I SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	-	-	6	40	60	100	3
CODE: 19MEC1LB01				**DESIGN AND SIMULATION LABORATORY**			

Course Objectives:

- Student able to design logic gates.
- Student able to learn about converters.
- Student able to understand the importance of embedded theory.

Course Outcomes:

By the end of the course, the student will be able to

- Design logic gates and ALU.
- Design Finite State Machine logic Circuit.
- Design Combinational circuits like Full Adder.
- Design A to D & D to A converters.
- Develop a new task.
- Implement BANKER'S algorithm.

PART-A:

VLSI Lab (Front-end Environment)

• The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).

• The students are required to acquire the knowledge in both the Platforms (Xilinx and Mentor graphics) by perform at least FOUR experiments on each Platform.

LIST OF EXPERIMENTS:

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter.
4. Synchronous RAM.
5. ALU.
6. UART Model.
7. Traffic Light Controller using Sequential Logic circuits
8. Finite State Machine (FSM) based logic circuit.

PART-B:

VLSI Lab (Back-end Environment)

• The students are required to design and implement the Layout of the following experiments of any THREE using CMOS 130nm Technology with Mentor Graphics Tool.

LIST OF EXPERIMENTS:

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Digital-to-Analog-Converter.
6. Analog-to-Digital Converter.

LAB REQUIREMENTS FOR PART-A AND PART-B:

Software: Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool.

Hardware: Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

PART-C: Embedded Systems Laboratory

• The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits.

• The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.

• The students are required to perform at least THREE experiments.

LIST OF EXPERIMENTS: (using ARM-926 with PERFECT RTOS)

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.

Lab Requirements for PART-C:

Software:

(i) Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library

(ii) LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

(i) The development kits of ARM-926 Developer Kits Boards.

(ii) Serial Cables, Network Cables and recommended power supply for the conduction of experiments.

I M.TECH-II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE:19MEC2TH01				**CODING THEORY AND APPLICATIONS**			

Course Objectives:

- Student able to differentiate the types of errors and error detection.
- Student able to compute and detect errors in cyclic and convolutional codes.
- Student able to compute Syndrome and iterative algorithms and error correcting codes.

Course Outcomes:

By the end of the course, the student will be able to

- Measure average and entropy.
- Implement Design hamming code.
- Compute cyclic hamming codes and shortened cyclic codes.
- Evaluate conventional codes like encoding of conventional codes.
- Decode single burst error correcting cyclic codes.
- Develop iterative algorithms.

UNIT –I

Coding for Reliable Digital Transmission and Storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

UNIT–II

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT–III

Cyclic Codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT–IV

Convolutional Codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT–V

Burst –Error-Correcting Codes: Decoding of Single-Burst error Correcting Cyclic codes, Single-Burst-Error-Correcting Cyclic codes, Burst-Error-Correcting Convolutional Codes,

Bounds on Burst Error- Correcting Capability, Interleaved Cyclic and Convolutional Codes, Phased-Burst –Error-Correcting Cyclic and Convolutional codes.

UNIT -VI

BCH – Codes: BCH code- Definition, Minimum distance and BCH Bounds, Decoding Procedure for BCH Codes- Syndrome Computation and Iterative Algorithms, Error Location Polynomials and Numbers for single and double error correction

TEXT BOOKS:

1. Shu Lin, Daniel J. Costello, Jr, "*Error Control Coding- Fundamentals and Applications*", Prentice Hall, Inc.
2. Man Young Rhee, "Error *Correcting Coding Theory*", McGraw-Hill Publishing, 1989.

REFERENCES:

1. Bernard Sklar, "*Digital Communications-Fundamental and Application*", PE.
2. John G. Proakis, "*Digital Communications*", 5th Ed., TMH, 2008.
3. Salvatore Gravano, "*Introduction to Error Control Codes*", Oxford.
4. Todd K.Moon, "*Error Correction Coding – Mathematical Methods and Algorithms*", Wiley India, 2006.
5. Ranjan Bose, "*Information Theory, Coding and Cryptography*", 2nd Ed., TMH, 2009.

I M.TECH-II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE2TH04				**DETECTION AND ESTIMATION THEORY**			

Course Objectives:

- Student able to know about discrete linear models and detection problem.
- Student able to discuss about importance of LMMSE Estimators and calculation of probability of error.
- Student able to measure non-parametric estimators and Model free estimation.

Course Outcomes:

By the end of the course, the student will be able to

- Interpret priority of Gaussian processes.
- Calculate probability of errors.
- Discuss the importance of minimum probability error with a priori probability.
- Design Kalman filters.
- Test hypotheses and linear regression.
- Estimate ergodicity and autocorrelation function

UNIT–I

Random Processes

Discrete Linear Models, Markov Sequences and Processes, Processes, and Gaussian Processes.

UNIT–II

Detection Theory

Basic Detection Problem, Maximum A posteriori Decision Rule, Minimum Probability of Error Classifier.

UNIT–III

Detection Methods

Bayes Decision Rule, Multiple-Class Problem (Bayes)- minimum probability error with and without equal apriori probabilities, Neyman-Pearson Classifier, General Calculation of Probability of Error, General Gaussian Problem, Composite Hypotheses.

UNIT–IV

Linear Minimum Mean-Square Error Filtering

Linear Minimum Mean Squared Error Estimators, Nonlinear Minimum Mean Squared Error Estimators. Innovations, Digital Wiener Filters with Stored Data, Real-time Digital Wiener Filters, Kalman Filters.

UNIT –V

Statistics

Measurements, Nonparametric Estimators of Probability Distribution and Density Functions, Point Estimators of Parameters, Measures of the Quality of Estimators, Introduction to Interval Estimates, Distribution of Estimators, Tests of Hypotheses, Simple Linear Regression, Multiple Linear Regression.

UNIT–VI

Estimating the Parameters of Random Processes from Data

Tests for Stationary and Ergodicity, Model-free Estimation, Model based Estimation of Autocorrelation Functions, Power Special Density Functions.

TEXT BOOKS:

1. K. Sam Shanmugan & A.M. Breipohl, "*Random Signals: Detection, Estimation and Data Analysis*", Wiley India Pvt. Ltd, 2011.
2. Lonnie C. Ludeman, "*Random Processes: Filtering, Estimation and Detection*" Wiley India Pvt. Ltd., 2010.

REFERENCES:

1. Steven. M.Kay, "*Fundamentals of Statistical Signal Processing: Volume I Estimation Theory*", Prentice Hall, USA, 1998.
2. Steven.M.Kay, "*Fundamentals of Statistical Signal Processing: Volume I Detection Theory*", Prentice Hall, USA, 1998.
3. Srinath, Rajasekaran, Viswanathan, "*Introduction to Statistical Signal Processing with Applications"*, PHI, 2003.
4. Louis L.Scharf, "*Statistical Signal Processing: Detection, Estimation and Time Series Analysis*", Addison Wesley, 1991.
5. Harry L. Van Trees, "*Detection, Estimation and Modulation Theory: Part – I*", John Wiley & Sons, USA, 2001.
6. Mischa Schwartz, Leonard Shaw, "*Signal Processing: Discrete Spectral Analysis – Detection & Estimation*", McGraw Hill, 1975.

I M.TECH-II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MEC2TH02				**DSP PROCESSORS AND ARCHITECTURES**			

Course Objectives:

- Gain concepts of digital signal processing techniques, implementation of DSP & FFT & their computational accuracies in DSP implementation.
- Understand the concepts of DSP Processor and its architectures and program a DSP processor to filter signals.
- Understand the concepts of various DSP device families & Interfacing of P-DSPs with Memory and peripherals

Course Outcomes:

By the end of the course, the student will be able to

- Comprehends the knowledge & concepts of digital signal processing techniques, basic building blocks, implementation of DSP & FFT algorithms
- Estimate their computational accuracies in DSP implementation.
- Design Programmable DSP devices
- Use the DSP processors TMS 320C 54XX for implementation of DSP algorithms & its interfacing techniques with various I/O peripherals.
- Use various Analog Device Family of DSP Devices
- Interface Memory and I/O Peripherals to DSP processors

UNIT–I

Introduction to Digital Signal Processing: Introduction, ADigital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT–II

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT–III

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT-IV

Programmable Digital Signal Processors: Commercial Digital signal processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of MS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts ofTMS320C54XX processors, Pipeline operation of TMS320C54XX Processors.

UNIT–V

Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Blackfin Processor - The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of HardwareProcessing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT -VI

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan, "*Digital Signal Processing*", Thomson Publications, 2004.
2. K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, *"A Practical Approach to Digital Signal Processing"*, New Age International, 2006/2009
3. Woon- SengGan, Sen M. Kuo, "*Embedded Signal Processing with the Micro Signal Architecture Publisher*", Wiley-IEEE Press, 2007

REFERENCES:

1. B. Venkataramani and M. Bhaskar, *"Digital Signal Processors, Architecture, Programming and Applications ",* TMH, 2002.
2. Jonatham Stein, "*Digital Signal Processing*", John Wiley, 2005.
3. Lapsley et al., "*DSP Processor Fundamentals, Architectures & Features*", S. Chand & Co. ,2000.
4. Digital Signal Processing Applications Using the ADSP-2100 Family, The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI.
5. Steven W. Smith, "*The Scientist and Engineer's Guide to Digital Signal Processing*", California Technical Publishing, ISBN 0- 9660176-3-3, 1997
6. David J. Katz and Rick Gentile, "*Embedded Media Processing*", Analog Devices, Newnes, ISBN 0750679123, 2005.

I M.TECH-II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE2TH05				**ADVANCED COMPUTER ARCHITECTURE**			

Course Objectives:

- The course focus on computer design, pipelining, RISC instruction set.
- To introduce dynamic scheduling, different ILP software Techniques.
- To discuss the concept of memory architecture, interconnection and intel architecture.

Course Outcomes:

By the end of the course, the student will be able to

- Know the classes of computers and new trends and developments in computer design.
- Discuss pipelining, RISC processor, cache memory performance.
- Analyze the various techniques to enhance a processors ability to exploit instruction level parallelism (ILP) and its challenges.
- Design the architecture of Very large instruction word (VLIW).
- Describe the concept of systematic and distributed shared memory architecture.
- Differentiate the performance of interconnection network and intel architecture.

UNIT -I

Fundamentals of Computer Design: Fundamentals of Computer design,Changing faces of computing and task of computer designer,Technology trends, Cost price and their trends, Measuring andreporting performance, Quantitative principles of computer design,Amdahl's law.Instruction set principles and examples- Introduction, Classifyinginstruction set-MEmory addressing- type and size of operands,Operations in the instruction set.

UNIT–II

Pipelines: Introduction, Basic RISC instruction set, Simpleimplementation of RISC instruction set, Classic five stage pipe linedRISC processor, Basic performance issues in pipelining, Pipelinehazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, Review of ABC of cache,Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT-III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling usingTomasulo's approach, Branch prediction, high performance instructiondelivery- hardware based speculation.

UNIT–IV

ILP Software Approach Basic compiler level techniques, Static branchprediction, VLIW approach, Exploiting ILP, Parallelism at compile time,Cross cutting issues -Hardware verses Software.

UNIT –V

Multi Processors and Thread Level Parallelism: Multi Processorsand Thread level Parallelism- Introduction, Characteristics ofapplication domain, Systematic shared memory architecture, Distributedshared – memory architecture, Synchronization.

UNIT–VI

Inter Connection and Networks: Introduction, Interconnection networkmedia, Practical issues in interconnecting networks, Examples of interconnection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets, Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.

REFERENCES:

1. Kai Hwang, Faye A. Brigs., "*Computer Architecture and Parallel Processing*", MC Graw Hill.
2. Dezso Sima, Terence Fountain, Peter Kacsuk , "*Advanced Computer Architecture – A Design Space Approach*", Pearson Ed.

I M.TECH-II SEMESTER **(ELECTIVE-III)**	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MEC2TH03				**CMOS ANALOG AND DIGITAL IC DESIGN**			

Course Objectives:

- Study the behavior of MOS Devices and Small-Signal & Large-Signal Modeling of MOS Transistor and Analog Sub-Circuits.
- Design concepts of Combinational and Sequential MOS logic circuits.
- Design concepts of Sub circuits and CMOS Amplifiers like Differential Amplifiers, Cascode Amplifiers, Output Amplifiers, and Operational Amplifiers.

Course Outcomes:

By the end of the course, the student will be able to

- Design MOS devices and estimate their Electrical behavior.
- Design Combinational MOS logic circuits.
- Design Sequential MOS logic circuits.
- Use the Dynamic logic circuits and Memories.
- Extend the Analog Circuit Design to Different Applications in Real Time.
- Measure characteristics of CMOS amplifiers.

UNIT-I

MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

MOS Design Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

Combinational MOS Logic Circuits

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT–III

Sequential MOS Logic Circuits

Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT–IV

Dynamic Logic Circuits

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Semiconductor Memories Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

UNIT–V

Analog CMOS Sub-Circuits

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT-VI

CMOS Amplifiers

nverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

CMOS Operational Amplifiers Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

TEXT BOOKS:

1. Ken Martin, "*Digital Integrated Circuit Design*", Oxford University Press, 2011.
2. Sung-Mo Kang, Yusuf Leblebici, "*CMOS Digital Integrated Circuits Analysis and Design*", 3rd Ed., TMH, 2011.
3. Philip E. Allen and Douglas R. Holberg, "*CMOS Analog Circuit Design*", Oxford University Press, International Second Edition/Indian Edition, 2010.
4. Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, "*Analysis and Design of Analog Integrated Circuits*", Fifth Edition, Wiley India, 2010.

REFERENCES:

1. David A. Johns, Ken Martin, "*Analog Integrated Circuit Design*", Wiley Student Edn, 2013.
2. Behzad Razavi, "*Design of Analog CMOS Integrated Circuits*", TMH Edition.
3. Baker, Li and Boyce, "*CMOS: Circuit Design, Layout and Simulation*", PHI.
4. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, *"Digital Integrated Circuits – A Design Perspective"*, 2nd Ed., PHI.

.

I M.TECH-II SEMESTER (ELECTIVE-III)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE2TH06				ADVANCED DIGITAL SIGNAL PROCESSING			

Course Objectives:

- Ability to study Signal processing at Different rates and its applications.
- Students able to implement Digital filters and able to estimate non-parametric methods.
- Students able to implement filter structures and able to estimate power spectrum of
- parametric methods.

Course Outcomes:

By the end of the course, the student will be able to

- Differentiate Decimation and interpolation.
- Design phase filters.
- Implement Quadrature Mirror filters.
- Estimate Welch and Blackman-Tukey methods.
- Implementation of structures of IIR filters.
- Estimate power spectrum of parametric methods like Yule-walker.

UNIT–I

Review of DFT, FFT, IIR Filters and FIR Filters:

Multi Rate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion.

UNIT–II

Applications of Multi Rate Signal Processing I:

Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters.

UNIT–III

Applications of Multi Rate Signal Processing II:

Implementation of Digital Filter Banks, Sub-band Coding of Speech Signals, Quadrature Mirror Filters, Trans-multiplexers, Over Sampling A/D and D/A Conversion.

UNIT-IV

Non-Parametric Methods of Power Spectral Estimation:

Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman-Tukey methods, Comparison of all Non-Parametric methods

UNIT–V

Implementation of Digital Filters:

Introduction to filter structures (IIR & FIR), Frequency sampling structures of FIR, Lattice structures, Forward prediction error, Backward prediction error, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT–VI

Parametric Methods of Power Spectrum Estimation:

Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation, Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXT BOOKS

1. J.G.Proakis and D. G. Manolakis, "*Digital Signal Processing: Principles, Algorithms and Applications*", 4th Ed., PHI.
2. Alan V Oppenheim & R. W Schaffer, "*Discrete Time Signal Processing*", PHI.
3. Emmanuel C. Ifeacher, Barrie. W. Jervis, "*DSP – A Practical Approach*", 2 Ed., Pearson Education.

REFERENCES:

1. S. M .Kay, "*Modern Spectral Estimation: Theory & Application*", PHI, 1988.
2. P.P.Vaidyanathan , "*Multi Rate Systems and Filter Banks*", Pearson Education.
3. S.Salivahanan, A.Vallavaraj, C.Gnanapriya, "*Digital Signal Processing*", TMH, 2000.

I M.TECH-II SEMESTER (ELECTIVE-III)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE2TH07				**RF CIRCUIT DESIGN**			

Course Objectives:

- The course focus on RF behavior of passive components and transmission lines.
- To introduce active components and RF transistor amplifier design.
- To discuss the concept of oscillators and RF mixers.

Course Outcomes:

By the end of the course, the student will be able to

- Discuss the concept of electromagnetic spectrum and microwave bands.
- Analyze the transmission line equations and smith chart.
- Interpret the various techniques to matching and biasing network.
- Design the transistor amplifier.
- Describe the concept of different types oscillators.
- Evaluate the performance of RF mixers.

UNIT-I

Introduction to RF Electronics: The Electromagnetic Spectrum, units and Physical Constants, Microwave bands – RF behavior of Passive components: Tuned resonant circuits, Vectors, Inductors and Capacitors - Voltage and Current in capacitor circuits – Tuned RF / IF Transformers.

UNIT-II

Transmission Line Analysis: Examples of transmission lines, Transmission line equations and Biasing- Micro Strip Transmission Lines- Special Termination Conditions- sourced and Loaded Transmission Lines. Single And Multiport Networks: The Smith Chart, Interconnectivity networks, Network properties and Applications, Scattering Parameters.

UNIT-III

Matching and Biasing Networks: Impedance matching using discrete components – Micro strip line matching networks, Amplifier classes of Operation and Biasing networks. RF Passive & Active Components: Filter Basics – Lumped filter design – Distributed Filter Design – Diplexer Filters- Crystal and Saw filters- Active Filters - Tunable filters – Power Combiners / Dividers – Directional Couplers – Hybrid Couplers – Isolators. RF Diodes – BJTs- FETs- HEMTs and Models.

UNIT-IV

RF Transistor Amplifier Design: Characteristics of Amplifiers - Amplifier Circuit Configurations, Amplifier Matching Basics, Distortion and noise products, Stability Considerations, Small Signal amplifier design, Power amplifier design, MMIC amplifiers, Broadband High Power multistage amplifiers, Low noise amplifiers, VGA Amplifiers.

UNIT-V

Oscillators: Oscillator basics, Low phase noise oscillator design, High frequency Oscillator configuration, LC Oscillators, VCOs, Crystal Oscillators, PLL Synthesizer, and Direct Digital Synthesizer.

UNIT-VI

RF Mixers: Basic characteristics of a mixer - Active mixers- Image Reject and Harmonic mixers, Frequency domain considerations.

TEXT BOOKS:

1. Reinhold Ludwing, Pavel Bretchko, "*RF Circuit design: Theory and applications*", Pearson Education Asia Publication, New Delhi 2001.
2. Devendra K. Misra, "*Radio Frequency and Microwave Communication Circuits – Analysis and Design*" , Wiley Student Edition, John Wiley & Sons

REFERENCES:

1. Mathew M.Radmangh, "*Radio frequency and Microwave Electronics*", 2001, PE Asia Publ.
2. Christopher Bowick, Cheryl Aljuni and John Biyler, "*RF Circuit Design*", Elsevier Science, 2008.
3. Joseph Carr, "*Secrets of RF Design*", 3rd Edition, Tab Electronics.
4. Cotter W. Sawyer, "*Complete Wireless Design*", 2nd Edition, Mc-Graw Hill.

I M.TECH-II SEMESTER **(ELECTIVE-III)**	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE2TH08				**EMBEDDED C**			

Course Objectives:

- To learn the basic concepts of C programming and to learn the basic concepts of 8051 IO Interfacing
- To learn the objective oriented programming with C and to learn the hardware and software delay creations
- To learn with the example case study and to learn the applications of embedded c language

Course Outcomes:

By the end of the course, the student will be able to

- Discuss the basic c programming
- Interpret the basic Embedded C programming
- Analyze the 8051 IO Port programming
- Develop small embedded projects

UNIT–I

Programming Embedded Systems in C: Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions.

UNIT–II

Introducing the 8051 Microcontroller Family: Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions

UNIT–III

Reading Switches: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), the need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions

UNIT–IV

Adding Structure to the Code: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions

UNIT–V

Meeting Real-Time Constraints: Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions

UNIT–VI

Case Study: Intruder Alarm System: Introduction, The software architecture, Key software Components used in this example, running the program, the software, Conclusions

TEXT BOOKS:

1. Michael J. Pont, "*Embedded C*", Pearson Education.

REFERENCES:

1. Nigel Gardner, *"PIC Micro MCU C - An Introduction to Programming, The Microchip PIC in CCS C".*
2. Biswas, "*ATM Fundamentals*", Adventure books publishers, 1998.

I M.TECH-II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
(ELECTIVE-III)	4	-	-	40	60	100	3
CODE: 19MDE2TH12				**ANTENNAS FOR WIRELESS COMMUNICATION**			

Course Objectives:

- To gain an idea and experience with smart antenna environments, algorithms and implementation. Implementations of smart antennas, apply to modern cellular systems, wireless LAN's, radar, GPS, direction finding systems and others.
- To enable the student to synthesize and analyze wireless and mobile cellular communication systems over a stochastic fading channel.
- To be acquainted with different advanced multiple access and diversity reception techniques.
- To gain knowledge on digital cellular systems (GSM, modulation methods; FDMA, TDMA, and CDMA techniques).

Course outcomes:

By the end of the course, the student will be able to

- Analyze, work and design wireless and mobile cellular systems.
- Evaluate a system requirement for implementation of an appropriate Smart Antenna implementation. Understand how adaptive arrays can be applied to modern communication systems and remote sensing systems.
- Design a smart antenna or sensor system and be able to evaluate performance. Gain an understanding of the operation and application of spatial filtering accomplished by adaptive array antenna systems.

UNIT-I

Essential Techniques in Wireless Antenna Design & Systems**:** Evolution of Wireless Communication, Technologies in Mobile Communications, Antenna Design- Requirements for Mobile Antennas, Diversity Techniques. Land Mobile Antenna Design- Base Station Antenna Techniques – Types- Recent Base Station Antennas for Cellular Systems- Antennas for Personal Phone.

UNIT–II

Smart Antennas**:** Key Benefits, Smart Antenna Technology, Fixed & Switched Beam Forming, Adaptive Antenna, Adaptive Array for Wireless Local Loop Wideband Smart Antenna-Spatial Diversity-Diversity Combining-Coherent & noncoherent CDMA Spatial Processors, Dynamic Rescoring Using Smart Antennas, Beam Forming for CDMA, Digital Beam Forming.

UNIT–III

Antennas for Pagers, Portable Phones, RFID and Personal Communication**:** Pager Antenna-Practical Requirements-Effect of the Human Body on Antennas, Types and Performance, Portable Phone Antenna-Design Techniques-Antenna types.

UNIT–IV

Antennas for RFID and Personal Communication**:** Handsets- Design Concept-Antennas for GSM, PDC and PHS, Diversity Performance in PDC Handsets, RFID Antenna.

UNIT-V

Antennas for Cars**,** Trains, Intelligent Transportation*:* Antennas for Broadcast Reception in Cars, TV Reception in Cars, Train Radio System, Intelligent Transportation Systems, Vehicle Antennas, Omni Directional and Directional Antennas for Mobile Satellite.

UNIT-VI

Antennas for Mobile Satellite and Aeronautical mobile system*:* Antenna Systems for GPS, Array Antenna for GPS Reception, Handset Antennas for Satellite Systems Advanced Circularly Polarized Antennas-Crossed-Dipole Antennas, Crossed-Slot Antennas, Quadrifilar Helical Antennas, Micro strip Patch Antennas.

TEXT BOOKS:

1. Joseph C.Liberti & Theodore S. Rappaport, "Smart Antennas for Wireless Communication", Prentice Hall Communication Engineering Series.1999
2. K.Fujimoto, J.R.James, "Mobile Antenna Systems Handbook", Artech House 2nd edition, 2001.

REFERENCES:

1. Balanis.A, "Antenna Theory Analysis and Design", John Wiley and Sons, New York, 2000.
2. Kin-Lu Wang, "Planar Antenna for Wireless Communications", John-Wiley 2002.

I M.TECH-II SEMESTER **(ELECTIVE-IV)**	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE2TH09					**VLSI DESIGN AUTOMATION**		

Course Objectives:

- Student will discuss the basic concepts of CAD design using algorithms.
- Student will impart the knowledge in Modeling and Simulation of Digital Circuits.
- Student will evaluate the different Logic Synthesis and its verification.

Course Outcomes:

By the end of the course, the student will be able to

- Modify the CAD design problems using algorithmic paradigms
- Illustrate Backend Design Concepts
- Illustrate about Modeling and Simulation of Digital Circuits
- Summarize about different Logic Synthesis and its verification
- Analyze physical design problems of FPGA, MCM

UNIT-I

PRELIMINARIES& GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems

General Purpose Methods for Combinational Optimization: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT- II

LAYOUT COMPACTION: Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint –graph Compaction.

Placement and Partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithms, Partitioning

Floor Planning: Floor Planning Concepts, Shape Functions and Floor plan Sizing

Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing.

UNIT- III

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level modeling and simulation.

UNIT- IV

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary –Decision diagram, Two – Level Logic Synthesis. High Level Synthesis: Hardware Models, Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling

Algorithms, Some aspects of Assignment problem, High – level Transformations.

UNIT- V

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's partitioning and routing for segmented and staggered models.

UNIT- VI

Physical Design Automation of MCM's: MCM technologies, MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing –Maze routing, Multiple stage routing, Topologic routing, Integrated Pin –Distribution and routing, routing and programmable MCM's.

TEXT BOOKS:

1. S.H.Gerez, ―Algorithms for VLSI Design Automation‖, WILEY student edition, Johnwiley& Sons (Asia) Pvt.Ltd. 1999.
2. NaveedSherwani, ―Algorithms for VLSI Physical Design Automation‖, Springer International Edition 3rd edition, , 2005

REFERENCES:

1. Hill &Peterson, ―*Computer Aided Logical Design with Emphasis on VLSI*‖, John Wiley, 1993.
2. Wayne Wolf, ―*Modern VLSI Design: Systems on silicon*‖, Pearson Education Asia,2ND Edition, 1998.

I M.TECH-II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
(ELECTIVE-IV)	4	-	-	40	60	100	3
CODE: 19MDE2TH10				**NANO TECHNOLOGY**			

Course Objectives:

- Student will discuss the basic concepts of nanofabrication methods.
- Student will impart the knowledge in characterization methods for nanomaterials.
- Student will develop the application to biomedical engineering.

Course Outcomes:

By the end of the course, the student will be able to

- Identify and compare state-of-the-art nanofabrication methods and perform a critical analysis.
- Design processing conditions to engineer functional nanomaterials.
- Discuss and evaluate state-of-the-art characterization methods for nanomaterials, and determine nanomaterial safety and handling methods required during characterization.
- Explain the fundamental principles of nanotechnology and their application to biomedical engineering

UNIT-I

Atomic structure: Basic crystallography, Crystals and their imperfection, Diffusion, Nucleation and crystallization, metals, Semiconductor & Insulators, Phase transformation, Ceramic materials.

UNIT-II

Physical properties of materials: Electrical &Thermal properties, Optical properties of material, magnetic properties of materials, Density of state, Coulomb blockade, Kondo effect, Hall effect, Quantum hall Effect.

UNIT-III

Nanostructure1: Introduction to Nanotechnology, Zero dimensional Nanostructure – Nano particles, One Dimensional Nanostructue – Nano wires & Nano rods

UNIT-IV

Nanostructure2: Two Dimensional Nano structure-Films, Special Nano materials, Nano structures fabricated by physical techniques, Properties of Nano materials,application of Nano structure, Basics of Nano Electronics.

UNIT-V

Characterization of Nano materials: SPM Techniques – Scanning Tunneling Microscopy, Atomic force Microscopy, Magnetic force Microscopy, Electron Microscopy – Scanning Electron Microscope, Transmission Electron Microscope.

UNIT-VI

Nanobiotechnology: Nanobiomaterials and biocompatibility, structural & functional principles of bio nanotechnology, protein and dna based nanostructures, nanobio-analytics, nanotechnology in food, medicine and health science

TEXT BOOKS:

1. Introduction to solid state physics : C .Kittel
2. Introduction to theory of Solids : H.M. Roenberg

Reference Books:

1. Physics & Chemistry of materials : Joel I. Gersten
2. Handbook of Nanotechnology : Bharat Bhushan

I M.TECH-II SEMESTER (ELECTIVE–IV)	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	4	-	-	40	60	100	3
CODE: 19MDE2TH11				**ADVANCED DIGITAL COMMUNICATION**			

Course Objectives:

- To discuss the digital passband transmission and different types of digital modulation techniques.
- To analyze the different channel coding techniques and design considerations of a digital communication system.
- To analyze spread spectrum communication system.

Course Outcomes:

By the end of the course, the student will be able to

- Discuss the performance of a pass band digital communication system in terms of error rate and spectral efficiency.
- Interpret performance of various digital modulation techniques.
- Explain performance of various channel coding techniques.
- Differentiate the time and frequency domain analysis of the signals in a digital communication system.
- Design of digital communication system.
- Analyze performance of spread spectrum communication system.

UNIT-I

Digital Passband Transmission

Introduction, Pass band Transmission Model, Gram-Schmidt Orthogonalization Procedure, Geometric Interpretation of Signals, Response of Bank of Correlators to Noisy Input, Coherent Detection of Signals in Noise, Probability of Error, Correlation Receiver, Detection of Signals with unknown Phase.

UNIT-II

Digital Modulation Techniques I

Hierarchy of Digital Modulation Techniques, Coherent Binary PSK, Coherent Binary FSK, Coherent Quadriphase-Shift Keying, Coherent Minimum Shift Keying, Noncoherent Orthogonal Modulation, Noncoherent Binary Frequency-Shift Keying.

UNIT-III

Digital Modulation Techniques II

Differential Phase-Shift Keying, Comparison of Binary and Quaternary Modulation Schemes, M-ary Modulation Techniques, Power Spectra, Band-width Efficiency, Synchronization.

UNIT-IV

Channel Coding

Introduction, Discrete Memory less Channels, Linear Block Codes, Cyclic Codes, Convolution Codes, Maximum Likelihood Decoding of Convolution codes, Trellis-Coded Modulation, Coding for Compounded-Error Channels.

UNIT-V

Design Considerations Of A Digital Communication System

Intersymbol Interference, Nyquist's Criterion for Distortionless Baseband Binary Transmission, Correlative-Level Coding, Error Probability Plane, Bandwidth Efficiency Plane, Modulation and coding tradeoffs, defining, designing, and evaluating digital communication system, Modulation and coding for band limited channels.

UNIT-VI

Spread Spectrum Techniques

Pseudo noise sequences, Direct sequence Spread Spectrum systems, Frequency hopping systems, Synchronization and Jamming Considerations.

TEXT BOOKS:

1. Simon Haykin, "Digital communication", Third Edition, John Wiley and Sons.
2. B.Sklar, "Digital Communications", Second Edition, Pearson Education Asia. (Units II & IV)

REFERENCE BOOKS:

1. J.G. Proakis, "Digital Communications", Third Edition, McGraw Hill.
2. Biswas, "*ATM Fundamentals*", Adventure books publishers, 1998.

I M.TECH-II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
(ELECTIVE–IV)	4	-	-	40	60	100	3
CODE: 19MDE2TH13				**ADVANCED MICROPROCESSOR & MICROCONTROLLERS**			

Course Objectives:

- To familiarize the students with architecture of advanced microprocessors and microcontrollers.
- To introduce the programming concepts of processors.
- To expose the students to various interfacing devices with advanced microprocessors and microcontrollers.
- To introduce the concepts of interrupt mechanism.

Course Outcomes:

By the end of the course, the student will be able to

- Explain the architecture of advanced microprocessors and microcontrollers.
- Demonstrate programming proficiency using Instruction set.
- Analyze concept of interfacing different peripheral devices with advanced microprocessors and microcontrollers.
- Interpret the memory organization and I/O management of advanced microprocessors and microcontrollers.
- Summarize various interfacing and applications of advanced microprocessors and microcontrollers.

UNIT-I

Design of basic microprocessor architectural Concepts: Microprocessor architecture, word Lengths, addressable memory, Microprocessor's speed architectural characteristics, registers, instruction, memory addressing architecture ,ALU, GPR's Control logic & internal data bus.

UNIT-II

Microprocessor Instructions &Communication: Instruction Set ,Mnemonics, Basic Instruction Types , Addressing modes ,Microprocessor I/O connecting I/O put to Microprocessor ,Polling and Interrupts, Interrupt and OM. Controllers.

UNIT-III

Microcontroller: Introduction 8051 architecture and programming model. Internal RAM and registers, I/O ports, Interrupt system &Instruction sets.

UNIT-IV

Advanced Micro processors: lntel X86 family of advanced Microprocessor, programming model for 86 family. X86 addressing modes, instruction set, hardware of 186, 286, 386, 486 & Pentium processors. Motorola 68 XXX family of microprocessor, 68 XXX addressing modes, instruction set, hardware.

UNIT-V

Microprocessor 110: Data Communication, parallel I/O serial communication, Serial interface and UART, modems, I/O devices, D/A,A/D interface, special I/O devices.

UNIT-VI

Developing Microprocessor Based Products: Introduction to the Design Process, Preparing the specifications, Developing a design, Implementing and Testing and design, Regulatory Compliance Testing, design tool for Microprocessor Development.

Text Books:

1. C.M. Gilmore, "Microprocessors Principals and Application", MGH
2. Rajkamal, "Embedded System, Architecture &Programming",TMH

Reference Books:

1. Berry B. Berry, " Inter Series of microprocessors", PHI
2. D. V. Hall, "Microprocessor &Interfacing", TMH
3. Peatman, "Microprocessor Based System Design", Pearson

I M.TECH-II SEMESTER	L	T	P	INTERNAL MARKS	EXTERNAL MARKS	TOTAL MARKS	CREDITS
	-	-	6	40	60	100	3
CODE: 19MDE2LB01				**ADVANCED COMMUNICATIONS LABORATORY**			

Course Objectives:

- To obtain the Bit error rate using binary data
- Verify the various transforms on a given image
- To implement the FIR and IIR filter using DSP trainer Kit
- To study the ISDN training system with protocol analyzer

Course Outcomes:

By the end of the course, the student will be able to

- Obtain the Bit error rate using binary data.
- Verify the FIR and IIR filter using DSP trainer Kit.
- Study the ISDN training system with protocol analyzer.
- Determined the various losses present in optical fiber.
- Determined the output of a convolution of encoder and decoder for a given sequence

Note:

1. Minimum of 10 Experiments have to be conducted

2. All Experiments may be Simulated using MATLAB and to be verified using related training kits.

1. Measurement of Bit Error Rate using Binary Data
2. Verification of minimum distance in Hamming code
3. Determination of output of Convolutional Encoder for a given sequence
4. Determination of output of Convolutional Decoder for a given sequence
5. Efficiency of DS Spread- Spectrum Technique
6. Simulation of Frequency Hopping (FH) system
7. Effect of Sampling and Quantization of Digital Image
8. Verification of Various Transforms (FT / DCT/ Walsh /Hadamard) on a given Image (Finding Transform and Inverse Transform)
9. Point, Line and Edge detection techniques using derivative operators.
10. Implementation of FIR filter using DSP Trainer Kit (C-Code/Assembly code)
11. Implementation of IIR filter using DSP Trainer Kit (C-Code/ Assembly code)
12. Determination of Losses in Optical Fiber
13. Observing the Waveforms at various test points of a mobile phone using Mobile Phone Trainer
14. Study of Direct Sequence Spread Spectrum Modulation & Demodulation using CDMA-DSS BER Trainer
15. Study of ISDN Training System with Protocol Analyzer
16. Characteristics of LASER Diode.

***